R 15 - ACADEMICREGULATIONS (CBCS) FOR M. Tech. (REGULAR) DEGREE PROGRAMMES

Applicable for the students of M. Tech. (Regular) programme from the Academic Year ***2015-16*** and onwards

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the programme and who fulfill all the requirements for the award of the Degree.

1. ELIGIBILITY FOR ADMISSIONS

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2. AWARD OF M. Tech. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years, failing which he shall forfeit his seat in M. Tech. programme.

2.2 The student shall register for all 88 credits and secure all the 88 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 COURSES OF STUDY

The following specializations are offered at present for the M. Tech. programme of study.

1. Computer Science and Engineering
2. Machine Design
3. Power Electronics and Electrical Drives
4. Structural Engineering
5. VLSI System Design
6. Embedded Systems

4 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course

Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students with in 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5 ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%)in each semester shall be granted by the College Academic Committee on genuine medical grounds and valid reasons on representation by the candidate with supporting evidence.

5.3 Shortage of Attendance below65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fees hall be payable towards condonation of shortage of attendance.

5.6 A candidate shall get minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M.Tech Degree, The candidate shall complete all the academic requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

6.1 For the theory subjects 60 marks shall be awarded for the performance in the Semester End Examination and 40 marks shall be awarded for Continuous Internal Evaluation (CIE). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes with Part A as compulsory question (10 marks) consisting of 5 sub-questions carrying 2 marks each, and Part B with 3 questions to be answered out of 5 questions, each question carrying 10 marks. The details of the Question Paper pattern for End Examination (Theory) are given below:

- The Semester End Examination will be conducted for 60 marks. It consists of two parts. i).Part-A for 20 marks, ii). Part-B for 40 marks.

- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 4 marks each.

- Part-B to be answered 5 questions carrying 8 marks each. There will be two questions from each unit and only one should be answered.

6.2 For practical subjects, 60 marks shall be awarded for performance in the Semester End Examinations and 40 marks shall be awarded for day-to-day performance as Internal Marks.

6.3 The practical end semester examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed by the Principal from the panel of examiners recommended by Chairman, Board of Studies in respective Branches.

6.4 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.5 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Head of the Department shall be associated with the conduct of the Comprehensive Viva-Voce through a Committee. The Committee consisting of Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Principal from the panel of 3 examiners recommended by Chairman, Board of Studies in respective Branches. There are no internal marks for the Comprehensive Viva-Voce and evaluates for maximum of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.7 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to reappear for the Semester End Examination in that subject.

6.8 A candidate shall be given one chance to re-register for the subjects if the internal marks secured by a candidate is less than 50% and failed in that subject for maximum of two subjects and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in

the previous attempt stands cancelled.

6.9 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the Semester End Examination in that subject. He shall re-register for the subject when next offered.

7. Examinations and Assessment - The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
80% and above (≥ 80%, ≤ 100%)	O (Outstanding)	10
Below 80% but not less than 70% (≥ 70%, < 80%)	**A^+** (Excellent)	9
Below 70% but not less than 60% (≥ 60%, < 70%)	**A** (Very Good)	8
Below 60% but not less than 55% (≥ 55%, < 60%)	**B^+** (Good)	7
Below 55% but not less than 50% (≥ 50%, < 55%)	**B** (Above Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	Ab	0

7.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the

Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'Ab' Grade will be allocated in any Subject shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Subject/ Course only when he **gets GP≥6(B Grade or above).**

7.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\textbf{SGPA} = \left\{\sum_{i=1}^{N} C_i G_i\right\} / \left\{\sum_{i=1}^{N} C_i\right\} \textbf{ For each Semester},$$

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C is the no. of Credits allotted to the ith Subject, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

7.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

CGPA = $\left\{\sum_{j=1}^{M} C_j G_j\right\} / \left\{\sum_{j=1}^{M} Cj\right\}$ **… for all S Semesters registered**

(ie., upto and inclusive of S Semesters, $S \geq 2$ **),**

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), C is the no. of Credits allotted to the jth Subject, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

7.11 For Calculations listed in Item 7.6 – 7.10, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/ Courses will also be included in the multiplications and summations.

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

8.8 For Project work **Review I** in II Year I Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review I. If he fails to fulfill minimum marks, he has to reappear as per the recommendations of PRC.

8.9 For Project work **Review II** in II Year II Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review II. If he fails to fulfill minimum marks, he has to reappear as per the recommendations of PRC.

8.10 For Project Evaluation (Viva Voce) in II Year II Sem. there is an external marks of 150 and the same evaluated by the External examiner appointed by the Institution. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

8.11 If he fails to fulfill as specified in 8.10, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.12 The thesis shall be adjudicated by one examiner selected by the Institution. For this, Chairmen, BOS of the respective departments shall submit a panel of 3 examiners, who are eminent in that field with the help of the concerned guide and senior faculty of the department.

8.13 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is un favourable again, the thesis shall be summarily rejected.

8.14 If the report of the examiner is favourable, Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.15 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva- Voce examination.

9. AWARD OF DEGREE AND CLASS

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **88** Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤CGPA < 7.75
Second Class	6.00≤CGPA < 6.75

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

11. TRANSITORY REGULATIONS

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of two earlier or equivalent
subjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same
subject; otherwise, he has to identify an equivalent subject as per R15 Academic
Regulations.

12 GENERAL

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the Decision of the Academic Council is final.

12.6 The Academic Council may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Academic Council.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm, computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The hall ticket of the candidate is to be cancelled and sent to the controller of examinations, ANURAG ENGINEERING COLLEGE.

3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination(including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant-Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any office relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subjects and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders. They will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all semester

		examinations. The continuation of the course by the candidate is subject to the academic regulation in connection with forfeiture of seat.
8.	Posses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with college indulges in any malpractice or improper conduct mentioned in clause 6 to 8	Student of the college's expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeiture the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.

11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of the semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Malpractices committee, ANURAG ENGINEERING COLLEGE for further action to award suitable punishment.	

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M.TECH (VLSI SYSTEM DESIGN)

COURSE STRUCTURE AND SYLLABUS

I Year I Semester

Sub.. Code	Category	Subject	L	P	C
A31034	Core course I	VLSI Technology and Design	4	--	4
A31035	Core course II	CMOS Analog Integrated Circuit Design	4	--	4
A31036	Core course III	CMOS Digital Integrated Circuit Design	4	--	4
A31037	Core Elective I	Digital System Design	4	--	4
A31038		Hardware Software Co-Design			
A31039		Device Modeling			
A31040	Core Elective II	Advance Operating Systems	4	--	4
A31041		Micro Controllers for Embedded System Design			
A31042		Advanced Computer Architecture			
A31043	Open Elective I	CPLD and FPGA Architectures and Applications	4	--	4
A31044		Image and Video processing			
A31045		Software Defined Radio			
A31207	Laboratory I	VLSI Laboratory – I	--	4	2
A31208	Seminar I	Seminar	--	4	2
	Total		24	8	28

I Year II Semester

Sub. Code	Category	Subject	L	P	C
A32034	Core course IV	Low Power VLSI Design	4	--	4
A32035	Core course V	CMOS Mixed Signal Circuit Design	4	--	4
A32036	Core course VI	Design for Testability	4	--	4
A32037	Core Elective III	Scripting Languages	4	--	4
A32038		Digital Signal Processors and Architectures			
A32039		VLSI Signal Processing			
A32040	Core Elective IV	Optimization Techniques in VLSI Design	4	--	4
A32041		System On Chip Architecture			
A32042		Semiconductor Memory Design and Testing			
A32043	Open Elective II	CAD for VLSI Circuits	4	--	4
A32044		Coding Theory and Techniques			
A32045		Adhoc Wireless Networks			
A32207	Laboratory II	VLSI Laboratory – II	--	4	2
A32208	Seminar II	Seminar	--	4	2
	Total		24	8	28

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II Year I Semester

Subject Code	Category	Subject Name	L	P	C
A33207		Comprehensive Viva-Voce	-	-	4
A33208		Project work Review I	-	24	12
		Total Credits	-	24	**16**

II Year II Semester

Subject Code	Category	Subject Name	L	P	C
A34207		Project work Review II	-	8	4
A34208		Project Evaluation (Viva-Voce)		16	12
		Total Credits	-	24	16

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M.Tech I Year I Sem (VLSISD)	**L**	**T/P/D**	**C**
	4	**--**	**4**

VLSI TECHNOLOGY AND DESIGN

Course Objectives:

- Identify Different MOS Technologies, their fabrication process, trends and projections.
- Understand basic electrical properties, threshold voltage concepts in form of mathematical equations.
- Design of combinational networks, analyzation of power optimization, Apply these Concepts to Design validation.
- Need for clocking disciplines, methods, design validation and testing.
- understanding of Different Floor planning methods, Global Interconnect, Floor Plan Design, Off- chip connections.

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology:Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Course Outcomes:

After going through this course the student will be able to

- Apply fundamental knowledge of Fabrication process, Relations between the Vds and Ids, Gm,, Gds, Theresh hold voltage Vth.

- Learned about Various Design rules, Stick Diagrams and tools, Layout De sign tools.
- Understand or become aware of Static Complementary gates, Switch logics.
- Learned inter connect design, clocking disciplines, floor planning methods, how to Test different circuits.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. EshraghianEshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

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M.Tech I Year I Sem (VLSISD)	L	T/P/D	C
	4	--	4

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

Course Objectives:

- To understand the Basic MOS Device Physics.
- To understand the operation of different types of single stage amplifiers, current sources and current sinks and voltage references.
- To understand the analysis and design of analog circuits with emphasis on CMOS technology.
- To gain knowledge in designing of advanced operational amplifiers.
- To understand the fundamentals of comparators.

UNIT -I: MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II: Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III: CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV: CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V: Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Course Outcomes:

After going through this course the student will be able to

- Analyze how the simplified device models can be developed.
- Analyze and design current mirrors, differential amplifiers.
- Analyze and design advanced operational amplifiers.
- Analyze and design of comparators

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Course Objectives:

- Introduction to VLSI Systems
- CMOS logic Design,
- Combinational MOS logic circuits Circuit characterization and performance estimation
- Combinational and sequential circuit design
- Memory system design
- Design methodology and tools

UNIT –I: MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II: Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III: Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV: Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping,Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V: Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Course Outcomes:

After going through this course the student will be able to

- Be able to create models of moderately sized CMOS circuits that realize specified digital functions.
- Have an understanding of the characteristics of CMOS circuit construction.
- To introduce the concepts and techniques of modern integrated circuit design and testing (CMOS VLSI).
- Be able to design static CMOS combinational and sequential logic at the transistor level.

- Design for higher performance or lower area using alternative circuit families.
- Compare the tradeoffs of sequencing elements including flip-flops, transparent latches, and pulsed latches.
- Know memory units SRAMs, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandra kasan, Borivoje Nikolic, 2nd Ed., PHI.

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DIGITAL SYSTEM DESIGN
(ELECTIVE -I)

Course Objectives:
- Learn digital design using PLD's, BCD adder, shift and add multiplier.
- Learn state machines, Derivation, realization of SM charts ,serial adder and accumulator, Binary multiplier,Binary divider, realization with MUX.
- Learn Fault modeling and test pattern generation .
- Understand different methods for test pattern generation.
- Learn fault diagnosis in sequential Circuits.
- Understand machine identification and fault detection experiment .
- Understand circuit test approach, transition check approach.

Course Outcomes:
After going through this course the student will be able to
- Create understanding of the fundamental concepts of PLDs, design of FPGAs, logic's for sequence detectors.
- Learn basic techniques for designing circuits in electronic, communication and software systems.
- Develop skills in modeling and evaluating fault-modeling and test pattern generation. architectures in terms of reliability, availability and safety.

UNIT -I: Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II: Digital Design:
Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III: SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV: Fault Modeling& Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V: Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

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HARDWARE - SOFTWARE CO-DESIGN
(ELECTIVE -I)

Course Objectives:

- Describe an embedded system design flow from specification to physical realization
- View a system development holistically
- Master complex systems
- Describe structural behavior of systems
- Master contemporary development techniques
- Devise new theories, techniques, and tools in design, implementation and testing

UNIT –I: Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II: Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV: Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V: Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system

and lycos system.

Course Outcomes:

After going through this course the student will be able to

- Gain knowledge of contemporary issues and algorithms used.
- Understand the use of modern hardware/software tools for building prototypes of embedded systems
- Demonstrate practical skills in the construction of prototypes.
- Apply embedded software techniques to satisfy functional and response time requirements.
- Know the interfacing components, different verification techniques and tools.
- Understand different specification languages and integrate embedded hardware, software, and operating systems to meet the functional requirements of embedded applications.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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DEVICE MODELLING
(ELECTIVE -I)

Course Objectives:

- Introduce students to the physics of semiconductors and the inner working of semiconductor devices
- Provide students the insight useful for understanding new semiconductor devices and technologies.
- To learn the physics behind the semiconductor devices and study the various models.
- To understand the BJT, MOSFET and other semiconductor devices from the device perspective.

UNIT -I:

Introduction to Semiconductor Physics:

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices:

Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II:

Integrated Diodes:

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor:

Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:

Integrated MOS Transistor:

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics– MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:

VLSI Fabrication Techniques:

An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:

Modeling of Hetero Junction Devices:

Band gap Engineering, Band gap Offset at abrupt HeteroJunction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

Course Outcomes:

After going through this course the student will be able to

- Describe why the electrical conductivity is different for different materials
- Account for and calculate how the electrical conductivity varies with temperature, light and doping concentration for the semiconductors Si and GaAs
- formulate the basic principles and give examples of process technology that is used for fabricating semiconductor devices
- Analyze and describe the charge distribution in the pn diode and the MOS transistor for different bias voltages
- Analyze how different physical phenomena influence the current in semiconductor devices
- Calculate the current in the pn diode, the MOS transistor and the bipolar transistor using simplified device models based on the physical phenomena that influence the current
- Exemplify how the simplified device models can be developed to more complex models that deviate less from experimental data
- Describe how a complex device model can be implemented in a computer simulation
- Analyze the validity and determine the complexity that is needed in a computer model of a semiconductor devices for a certain application

TEXT BOOKS:

1 Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

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ADVANCED OPERATING SYSTEMS
(ELECTIVE -II)

Course Objectives:

- To study, learn, and understand the main concepts of advanced operating systems (parallel processing systems, distributed systems, real time systems, network operating systems, and open source operating systems); Hardware and software features that support these systems.
- Expose students to current operating systems literature
- Give students an understanding of what it means to do research in computer science and specifically operating systems
- Teach students to critically evaluate research papers

UNIT –I:

Introduction to Operating Systems:

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:

Introduction to UNIX and LINUX:

Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III:

System Calls:

System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication:

Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:

Introduction to Distributed Systems:

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:

Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:

Synchronization in Distributed Systems:

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:

Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Course Outcomes:

After going through this course the student will be able to

- Outline the potential benefits of distributed systems
- Summarize the major security issues associated with distributed systems along with the range of techniques available for increasing system security
- Apply standard design principles in the construction of these systems
- Select appropriate approaches for building a range of distributed systems, including some that employ middleware.
- Read and critique research papers
- Students will be familiar with current operating systems literature
- Students will make substantial contributions to a large operating systems project that can be submitted for publication

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

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MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN (ELECTIVE -II)

Course Objectives:

- To understand the Embedded Hardware Units and Devices in system, Embedded Software.
- To understand the resources of various microcontrollers and their programming concepts and interfacing of Memory and I/O devices.
- To understand the concepts of interrupts and ISRs .
- To understand the Network Protocols .

UNIT –I: ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II: ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III: ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV: ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V: Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

Course Outcomes:

After going through this course the student will be able to

- Select appropriate embedded software to design an embedded system.
- Design an embedded system using various microcontrollers.
- Design various device drivers for designing an embedded system.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

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ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE -II)

Course Objectives:

- Understanding the different instruction set formats, RISC and CISC and Various design issues for computers
- Introducing instruction level parallelism using software and hardware approaches.
- Learning multiprocessors and thread level parallelism.
- Discussing design issues for storage systems.
- Introducing the important concepts for interconnection networks and cluster.

UNIT -I: Fundamentals of Computer Design:
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set-memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II: Pipelines:
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III: Instruction Level Parallelism (ILP) - The Hardware Approach:
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery-Hardware based speculation.
ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV: Multi Processors and Thread Level Parallelism:
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V: Inter Connection and Networks:
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

Course Outcomes:

After going through this course the student will be able to

- Comparing different types of instruction sets
- Know the parallelism concepts used for increasing the efficiency of the computer and how it affects the cost of the system.
- Know the different types of networks, their interconnection and its components for interconnection.
- Understand the different types of storage devices and its internal structure. Apply all the ACA concepts to design the system efficiently.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk, Pearson Ed.

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Course objectives:

- To introduce the student to digital design using Field Programmable ICs, and to provide an under-standing of the underlying technologies and architectures of these Integrated Circuits.Underlying Field Programmable and Complex Programmable Logic IC architectures and technologies in detail.
- Structure of SRAM-based, Anti fuse- based & EPROM-based FPGAs and sample architectures
- Describing partitioning techniques to help logic synthesis provide the optimal logic network and also familiarize with the concepts of Placement and Routing algorithms for FPGAs
- Knowledge about EDA Tools for FPGAs & ASICs and specific case studies are presented.

UNIT-I: Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III: SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV: Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT -V: Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Course Outcomes:

After going through this course the student will be able to

- Classify programmable architectures.
- Comprehending FPGA and CPLD technologies
- Know how to minimize chip area, interconnect wire length, delays.
- Learn tools for implementing digital logic using a FPGA device.
- Build FPGA-based digital system.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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IMAGE AND VIDEO PROCESSING

UNIT –I:

Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II:

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III:

Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV:

Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V:

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.

2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Image Processing using MATLAB– Gonzaleze and Woods, 2 nd ed., Mc Graw Hill Education, 2010

2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE,2008

3. Digital Video Processing – A Murat Tekalp, PERSON, 2010

4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009

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SOFTWARE DEFINED RADIO

UNIT -I:

Introduction: The Need for Software Radios, What is Software Radio, Characteristics and benefits of software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front- End Topologies- Enhanced Flexibility of the RF Chain with Software Radios- Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

UNIT -II:

Profile and Radio Resource Management : Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

UNIT -III:

Radio Resource Management in Heterogeneous Networks

Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, CircuitSwitched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems.

UNIT -IV:

Reconfiguration of the Network Elements : Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration

Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT -V:

Object – Oriented Representation of Radios and Network Resources:

Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

Case Studies in Software Radio Design: Introduction and Historical Perspective, SPEAK easy- JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

TEXT BOOKS:

1. Software Defined Radio Architecture System and Functions- Markus Dillinger, Kambiz Madani, WILEY 2003

2. Software Defined Radio: Enabling Technologies- Walter Tuttle Bee, 2002, Wiley Publications.

REFERENCE BOOKS:

1. Software Radio: A Modern Approach to Radio Engineering - Jeffrey H. Reed, 2002, PEA

Publication.

2. Software Defined Radio for 3G - Paul Burns, 2002, Artech House.

3. Software Defined Radio: Architectures, Systems and Functions - Markus Dillinger, Kambiz

Madani, Nancy Alonistioti, 2003, Wiley.

4. Software Radio Architecture: Object Oriented Approaches to wireless System Enginering – Joseph Mitola, III, 2000, John Wiley & Sons.

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VLSI LABORATORY – I

Note: All the following digital circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs:

Programming can be done using any HDL complier, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
2. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with priority)
5. Design of 8-to-1 multiplexer and 1x8 Demultiplexer
6. Design of 4 bit binary to gray code converter
7. Design of 4-bit comparator
8. Design of flip flops: SR, D, JK, T
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
10. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in
    Serial out and Parallel in Parallel Out.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier and 4-bit Divider.
13. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplication and Division.
14. Design of Finite State Machine.

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LOW POWER VLSI DESIGN

Course Objectives:

To understand various power dissipation sources in VLSI design.

- To learn different Low-Power Design Approaches like Voltage Scaling and Switched
  Minimization Capacitance.
- To design the basic low power logic circuits and different adders using low power design techniques.
- To learn the design procedure of low power and low voltage multipliers.
- To design the low power and low voltage memories.

UNIT –I: Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II: Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, ArchitecturalLevel Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III: Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV: Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V: Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Course Outcomes:

After going through this course the student will be able to

- Know the different power dissipation sources in VLSI circuits and their significance in the system performance.
- Analyze the different Low-Power Design Approaches.
- Design the low power logic circuits and adders.
- Design the systems low power and low voltage multipliers.
- Analyze the performance of the digital systems in terms of low power and low voltage memories.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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CMOS MIXED SIGNAL CIRCUIT DESIGN

Course Objectives:

- To understand the switched capacitor circuits.
- To understand the basics of Phase Locked Loop (PLL).
- To understand the fundamentals and Design Architectures of data converters. (ADCs & DACs)

UNIT -I: Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II: Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III: Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters-Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV: Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V: Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

Course Outcomes:

After going through this course the student will be able to

- Analyze the switched capacitor circuits and PLL and its practical applications.
- Understand the design issues and challenges involved in data converters such as offset, noise, gain, bandwidth etc.
- Analyze and design different types of data converter architectures such as Nyquist Rate
- A/D Converters and Oversampling Converters.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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DESIGN FOR TESTABILITY

Course Objectives:

- Testing philosophy, role of testing, digital and VLSI Testing, Types of testing.
- Functional versus structural testing, levels of faults, Single stuck at fault models.
- Learn SCOAP controllability and observability, high level testability Measures.
- Understand testability AD HOC DFT methods, scan design, partial scan design.
- Learn design for testability concepts for combinational Circuits.
- Understand scan architectures & techniques, Scan based testing, functional testing.
- Learn test pattern generation for BIST exhaustive testing, pseudo random testing.

UNIT -I: Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, FaultModeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II: Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III: Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV: Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V: Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Course Outcomes:

After going through this course the student will be able to

- Create understanding of the fundamental concepts of Testing.
- Learn basic techniques for achieving fault-testing in electronic, communication and software systems.
- Develop skills in modeling and evaluating fault-testing architectures in terms of reliability, availability and safety.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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SCRIPTING LANGUAGES FOR VLSI
(ELECTIVE -III)

Course Objectives:

- Characteristics and uses of scripting languages , Names and values, Scalar expressions .
- Learn Collections of Data, Working with arrays , Lists and hashes, Strings, Patterns and regular expressions, Subroutines.
- Working with files, Navigating the file system.
- Understand Type globs, Eval, References, Data structures, Packages, Libraries and modules.
- Learn The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL.
- Understand The eval, source, exec and up-level commands, Libraries and packages,namespaces.
- Learn JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core .
- Object Oriented Programming Concepts: Objects, Classes, Encapsulation, Data Hierarchy

UNIT -I:

Introduction to Scripts and Scripting:

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II:

Advanced PERL:

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III:
TCL:

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with

Strings, Patterns, Files and Pipes, Example code.

UNIT -IV:

Advanced TCL:

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V:

TK and JavaScript:

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.
Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Course Outcomes:

After going through this course the student will be able to

- Explain the differences between typical scripting languages and typical system and application programming languages.
- Create software systems using scripting languages, including Perl and Python.
- Write server-side scripts using Perl and Python's CGI facilities.

TEXT BOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS:

1. Tcl/Tk: A Developer's Guide- ClifFlynt, 2003, Morgan Kaufmann Series.
2. Tcl and the Tk Toolkit- JohnOusterhout, 2nd Edition, 2009, Kindel Edition.
1. Tcl 8.5 Network Programming book- WojciechKocjan and PiotrBeltowski, Packt Publishing.
2. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(ELECTIVE -III)

Course Objectives:

- To study the Architectural details of TMS320C54xx DSPs and the concepts involved in execution control and pipelining
- To present clear idea of Number formats for signals and sources of errors in DSP implementation
- Memory & I/O interfacing for digital signal processors
- Implementations of basic DSP algorithms

Course Outcomes:

After going through this course the student will be able to

- Understand concepts of Digital signal processor, like its architecture, registers etc
- Writing programs using the instruction set of DSP processor
- Interfacing different devices to the processor.
- Understand all the peripherals existing on the DSP processor.
- Apply DSP processors in real time.
- Ability to analyze the DSP algorithm.

UNIT –I: Introduction to Digital Signal Processing:
Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.
Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II: Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III: Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX

Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV: Analog Devices Family of DSP Devices:
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.
Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V: Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
1. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
2. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
3. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
4. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

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VLSI SIGNAL PROCESSING
(ELECTIVE -III)

Course Objectives:
- To study various DSP algorithms and retiming concepts.
- To learn the concepts of folding and unfolding techniques
- To understand the concepts of systolic architecture design.
- To study fast convolution methods
- To study various power consumption methods in VLSI

UNIT -I: Introduction to DSP:
Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT –II: Folding and Unfolding:
Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimizationin folded architectures – folding of multirate systems
Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path,Unfolding and Retiming – Applications of Unfolding

UNIT -III: Systolic Architecture Design:
Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT -IV: Fast Convolution:
Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V: Low Power Design:
Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches
Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

Course Outcomes:
After going through this course the student will be able to
- Design the systems by using the appropriate DSP algorithms and Filter techniques.

- Analyze and design the folding and unfolding techniques in real time application.
- Design the systems by using systolic architectures.
- Design the systems by using various fast convolution algorithms
- Evaluate the performance of various digital signal processors in terms of low power dissipation

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(ELECTIVE -IV)

Course Objectives:

- Understand the trade offs among various design styles given a set of design constraints in physical design automation and to understand performance/area tradeoffs in a chip design process.
- Learn the implementation issues for digital design automation including optimization techniques.
- Understand concept of design optimization algorithms and their application to physical design automation.
- Understand the latest design techniques as practiced in the Indus try for design layout optimization.
- To understand the concepts of Physical Design Process such as Partitioning, Floor planning, Placement and Routing.

UNIT –I: Statistical Modeling:
Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom s model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II: Statistical Performance, Power and Yield Analysis:
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III: Convex Optimization:
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV: Genetic Algorithm:
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V: GA Routing Procedures and Power Estimation:
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

Course Outcomes:
After going through this course the student will be able to

- Apply the appropriate design practices, emerging technologies, state-of-the-art design techniques, software tools, and research methods for IC design.
- Design the systems by using concepts of High level statistical, Gate level statistical analysis methods.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using optimization techniques like Genetic Algorithms.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - AshishSrivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - PinakiMazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, LievenVandenberghe, Cambridge University Press, 2004.

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SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

Course Objectives:

- Understand the design concepts of processor, pipelining concepts
- Understand the Memory Hierarchy, cache design and Memory Management.
- Understand the architectural support for system development, AMBA Architecture, Hardware system prototyping tools and Debug architecture.

UNIT –I: Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III: Memory Design for SOC:
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV: Interconnect Customization and Configuration:
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V: Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Course Outcomes:

After going through this course the student will be able to

- Apply fundamental knowledge of digital logic design to modeling and analysis of low power problem in processor design.
- Write a program with ARM Instruction set and in 'C' Language for developing an application.
- Interface ARM with memory, peripheral systems and use the required operating system for designing an embedded system.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE -IV)

Course Objectives:

- To study different types memory architectures and their applications.
- To learn Non volatile memory designs.
- To study fault modeling techniques for memory design.
- To understand the effects of radiation on semiconductor memories.
- To learn various high density packages.

UNIT -I: Random Access Memory Technologies:
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II: Non-volatile Memories:
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:
RAMfault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV: Semiconductor Memory Reliability and Radiation Effects:
General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V: Advanced Memory Technologies and High-density Memory Packing Technologies:

FerroelectricRAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

Course Outcomes:

- After going through this course the student will be able to
- Describe the applications various memory architectures.
- Analyze the need of non-volatile memories and their applications.
- Design the fault free memory systems by fault modeling techniques.
- Analyze and design the memory architectures by considering the radiation affects.
- Design the advanced memory architectures

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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CAD FOR VLSI CIRCUITS

Course Objectives:

- Understand the VLSI design methodologies and VLSI design Automation tools.
- Emphasize the physical design problems , including partitioning, floor planning , placement and routing of VLSI circuits then identify and formulate CAD Design problems by using mathematical programming.
- Implement these algorithms by using 'C' Data structures.
- Apply these data structures to analyze problems by making good assumptions and learn systematic engineering method to solve practical CAD problems with FPGA .
- Apply fundamental principles of MCM Technologies to implement VLSI application.

UNIT -I: VLSI Physical Design Automation:

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT -II: Partitioning, Floor Planning, Pin Assignment and Placement:

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement **–** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT -III: Global Routing and Detailed Routing:

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT -IV: Physical Design Automation of FPGAs:

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

Physical Design Automation of MCMs:

Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT -V: Chip Input and Output Circuits:
ESD Protection, Input Circuits, Output Circuits and ΔI noise, On-chip clock Generation and
Distribution, Latch-up and its prevention.

Course Outcomes:

After going through this course the student will able to

- Apply fundamental knowledge of mathematics to modeling and analysis of CAD problems in VLSI circuits.
- Implement CAD algorithms using computer programming in FPGAs and conduct and interpreting data from model studies to prototype cases, as well as documenting them in engineering reports.
- Become familiar with the critical challenges in the physical design on VLSI circuits implement the System by using MCM technologies.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

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CODING THEORY AND TECHNIQUES

UNIT -I:

Coding for Reliable Digital Transmission and Storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT –II:

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT –III:

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT –IV:

Burst –Error-Correcting Codes: Decoding of Single-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convolutional Codes, Bounds on Burst Error-Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst –Error-Correcting Cyclic and Convolutional codes.

UNIT -V:

BCH – Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

TEXT BOOKS:

9. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall, Inc.
10. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill Publishing.

REFERENCE BOOKS:

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
2. Digital Communications- John G. Proakis, 5th Ed., 2008, TMH.
3. Introduction to Error Control Codes-Salvatore Gravano-Oxford
4. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.
5. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, 2009, TMH.

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M.Tech I Year II Sem (VLSISD)

ADHOC AND WIRELESS SENSOR NETWORKS

UNIT-I:

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11 Standard, HIPERLAN Standard, Bluetooth, Home RF.

Wireless Internet:

Wireless Internet, Mobile IP, TCP in Wireless Domain, WAP, Optimizing Web Over Wireless.

UNIT-II:

AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.

MAC Protocols for Ad Hoc Wireless Networks: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT -III:

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

Transport Layer and Security Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks, Security in Ad Hoc Wireless Networks, Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks, Key Management, Secure Routing in Ad Hoc Wireless Networks.

UNIT –IV:

Quality of Service: Introduction, Issues and Challenges in Providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions, MAC Layer Solutions, Network Layer Solutions, QoS Frameworks for Ad Hoc Wireless Networks.

Energy Management: Introduction, Need for Energy Management in Ad Hoc Wireless Networks, Classification of Ad Hoc Wireless Networks, Battery Management Schemes, Transmission Power Management Schemes, System Power Management Schemes.

UNIT –V:

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location

Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press

REFERENCE BOOKS:

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh ,1 ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

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VLSI LABORATORY – II

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - CMOS inverter
   - CMOS NOR/ NAND gates
     CMOS XOR and MUX gates
   - CMOS half adder and full adder
   - Static / Dynamic logic circuits (register cell)
     Latch
     Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL