ANURAG Engineering College

(Autonomous)

Ananthagiri (V & M), Kodad, Suryapet (Dt.). T.S. India. PIN: 508 206.

EXAMINATION BRANCH

TIME TABLE

I M.TECH I SEMESTER – REGULAR / SUPPLEMENTARY EXAMINATIONS (R15), DEC-2018/JAN – 2019

TIME→ AN: 10:00 AM TO 01:00 PM **Date : 10-12-2018**

BRANCH	DATE AND DAY					
	21-12-2018 FRIDAY	**27-12-2018 THURSDAY**	**29-12-2018 SATURDAY**	**31-12-2018 MONDAY**	**02-01-2019 WEDNESDAY**	**04-01-2019 FRIDAY**
Power Electronics and Electrical Drives (54 – PEED)	Machine Modeling and Analysis	Modern Control Theory	Power Electronic Control of DC Drives	Special Machines	HVDC Transmission	Power Electronic Converters-I
VLSI System Design (57 – VLSI SD)	VLSI Technology and Design	CMOS Analog Integrated Circuit Design	CMOS Digital Integrated Circuit Design	Digital System Design	Micro Controllers for Embedded System Design	CPLD and FPGA Architectures and Applications

NOTE: The students should occupy their seats 10 min before Commencement of the Examination.

PRINCIPAL

PRINCIPAL
ANURAG ENGINEERING COLLEGE
(Autonomous)
Ananthagiri(V&M), Suryapet Dt.,T.S.

To
HODs to circulate among their concerned Students and Faculty.
Department Notice Board
Examination Branch Notice Board
Administrative Office