ANURAG Engineering College

(Autonomous)

Ananthagiri (V & M), Kodad, Suryapet (Dt.). T.S. India. PIN: 508 206.

EXAMINATION BRANCH

T I M E T A B L E

I M.TECH II SEMESTER – REGULAR EXAMINATIONS (R15), JUN – 2019

TIME→ FN: 10:00 AM TO 01:00 PM **Date : 15-04-2019**

BRANCH	DATE AND DAY					
	17-06-2019 MONDAY	**19-06-2019 TUESDAY**	**21-06-2019 FRIDAY**	**24-06-2019 MONDAY**	**26-06-2019 WEDNESDAY**	**28-06-2019 FRIDAY**
Power Electronics and Electrical Drives (54 – PEED)	Power Electronic Converters – II	Neural Networks and Fuzzy Systems	Power Electronic Control of AC Drives	Power Quality	Flexible AC Transmission Systems	AI Techniques in Electrical Engineering
VLSI System Design (57 – VLSI SD)	Low Power VLSI Design	CMOS Mixed Signal Circuit Design	Design for Testability	Digital Signal Processors and Architectures	System On Chip Architecture	CAD for VLSI Circuits / Coding Theory and Techniques

NOTE: The students should occupy their seats 10 min before Commencement of the Examination.

PRINCIPAL

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ANURAG ENGINEERING COLLEGE
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Ananthagiri(V&M), Suryapet Dt.,T.S.

To
HODs to circulate among the concerned students and faculty.
Department Notice Board
Examination Branch Notice Board
Administrative Office