ANURAG ENGINEERING COLLEGE

(An Autonomous Institution)

IV Year B.Tech. ECE – I Sem   L   T/P/D   C
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(EC703PC) E-CAD & VLSI LAB

List of Experiments:

Design and implementation of the following CMOS digital/analog circuits using **Cadence /Mentor Graphics / Synopsys /Equivalent** CAD tools.

Note: Minimum of 12 experiments to be conducted.

E-CAD Programs:

Programming can be done by using any compiler.
 1. HDL code to realize all the logic gates.
 2. Design of 3-to -8 decoder.
 3. design of full adder using half adders
 4. design of binary adder
 5. Design of 4 bit binary to gray converter, gray to binary converter.
 6. Design of flips: SR, D, JK, T.
 7. Design of decade counter
 8. Finite state machine design

VLSI Program:

 1. Introduction to layout design rules:
    Schematic, Simulation, Layout design, physical verification analysis of following.
 2. CMOS inverter
 3. CMOS NOR/ NAND gates
 4. CMOS XOR/ MUX gates
 5. CMOS half adder/full adder
 6. Basic analog circuit - Differential Amplifier
 7. Analog Circuit simulation (AC analysis) – CS & CD amplifier
 8. Layout of any combinational circuit (complex CMOS logic gates)