ANURAG ENGINEERING COLLEGE

(An Autonomous Institution)

M.Tech I Year I Sem (VLSISD)	**L**	**T/P/D**	**C**
	--	**4**	**2**

VLSI LABORATORY – I

Note: All the following digital circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs:

Programming can be done using any HDL complier, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
1. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
2. Design of 2-to-4 decoder
3. Design of 8-to-3 encoder (without and with priority)
4. Design of 8-to-1 multiplexer and 1x8 Demultiplexer
5. Design of 4 bit binary to gray code converter
6. Design of 4-bit comparator
7. Design of flip flops: SR, D, JK, T
8. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
9. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in
   Serial out and Parallel in Parallel Out.
10. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
11. Design of 4- Bit Multiplier and 4-bit Divider.
12. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplication and Division.
13. Design of Finite State Machine.