

ANURAG ENGINEERING COLLEGE
(An Autonomous Institution)

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M.Tech I Year II Sem (VLSISD)

VLSI LABORATORY – II

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
 - CMOS inverter
 - CMOS NOR/ NAND gates CMOS XOR and MUX gates
 - CMOS half adder and full adder
 - Static / Dynamic logic circuits (register cell)
Latch
Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL