



ANURAG Engineering College

(Autonomous)

Ananthagiri (V & M), Kodad, Suryapet (Dt.). T.S. India. PIN: 508 206.

EXAMINATION BRANCH

I M.TECH I SEMESTER – REGULAR / SUPPLEMENTARY EXAMINATIONS (R15), JULY – 2021 TIME TABLE


TIME AN: 10:45 AM TO 01:45 PM

Date : 06-07-2021

BRANCH	DATE AND DAY					
	13.07.2021 TUESDAY	15.07.2021 THURSDAY	17.07.2021 SATURDAY	20.07.2021 TUESDAY	23.07.2021 FRIDAY	26.07.2021 MONDAY
Power Electronics and Electrical Drives (54 – PEED)	Machine Modeling and Analysis	Modern Control Theory	Power Electronic Control of DC Drives	Special Machines	HVDC Transmission	Power Electronic Converters-I
VLSI System Design (57 – VLSI SD)	VLSI Technology and Design	CMOS Analog Integrated Circuit Design	CMOS Digital Integrated Circuit Design	Digital System Design (Core Elective-I)	Micro Controllers for Embedded System Design (Core Elective-II)	CPLD and FPGA Architectures and Applications (Open Elective-I)

NOTE: The students should occupy their seats 10 min before Commencement of the Examination.

To
HODs to circulate among their concerned Students and Faculty.
Department Notice Board
Examination Branch Notice Board
Administrative Office


PRINCIPAL
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