Department of Electronics and Communication Engineering

Course File

ELECTRONIC CIRCUIT ANALYSIS

(Course Code: EC405PC)

II B.Tech II Semester

2023-24

Mrs. B.SWETHA
Assistant Professor

Ananthagiri, Kodad, Telangana 508 206, India.

ELECTRONIC CIRCUIT ANALYSIS

Check List

Int. Marks:40 Ext. Marks:60 Total Marks:100

ELECTRONIC CIRCUIT ANALYSIS

Course Code:EC405PC **L/T/P/C:3/0/0/3**
II Year II Semester

UNIT - I

Large Signal Amplifiers: Class A Power Amplifier- Series fed and Transformer coupled, Conversion Efficiency, Class B Power Amplifier- Push Pull and Complimentary Symmetry configurations, Conversion Efficiency, Principle of operation of Class AB and Class –C and D Amplifiers.

UNIT- II

Tuned Amplifiers: Introduction, single Tuned Amplifiers – Q-factor, frequency response, Double Tuned Amplifiers – Q-factor, frequency response, Concept of stagger tuning and synchronous tuning

UNIT - III

Multivibrators: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt triggerusing Transistors.

UNIT - IV

Time Base Generators: General features of a Time base Signal, Methods of Generating Time Base Waveform, concepts of Transistor Miller and Bootstrap Time Base Generator, Methods of Linearity improvement.

UNIT - V

Synchronization and Frequency Division: Pulse Synchronization of Relaxation Devices, Frequency division in Sweep Circuits, Stability of Relaxation Devices, Astable Relaxation Circuits, Monostable Relaxation Circuits, Synchronization of a Sweep Circuit with Symmetrical Signals, Sine wave frequency division with a Sweep Circuit, A Sinusoidal Divider using Regeneration and Modulation.

Sampling Gates: Basic operating principles of Sampling Gates, Unidirectional and Bi-directional Sampling Gates, Four Diode Sampling Gate, Reduction of pedestal in Gate Circuits

TEXT BOOKS:

1. Jacob Millman, Christos C Halkias - Integrated Electronics, , McGraw Hill Education.
2. J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital andSwitching Waveforms –2nd Ed., TMH, 2008,

REFERENCE BOOKS:

1. David A. Bell - Electronic Devices and Circuits, 5th Ed., Oxford.
2. Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuitstheory, 11th Ed.,Pearson, 2009
3. Ronald J. Tocci - Fundamentals of Pulse and Digital Circuits, 3rd Ed., 2008.
4. David A. Bell - Pulse, Switching and Digital Circuits, 5th Ed., Oxford, 2015.

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Timetable

II B.Tech. II Semester –ECA (A&B Sections)

Day/Hour	09:30AM - 10:20AM	10:20AM- 11:10AM	11:20AM- 12:10 PM	12:10 PM - 01:00 PM	01:40 PM - 02:25PM	02:25 PM- 03:10 PM	03:15 PM- 04:00 PM
Monday		ECE-B	ECE-B		ECE-A		
Tuesday			ECE-A	ECE-B			
Wednesday	ECE-A				ECE-B		
Thursday						ECE-A	ECE-B
Friday							
Saturday		ECE-A		ECE-B			

Vision of the Institute

To be a premier Institute in the country and region for the study of Engineering, Technology and Management by maintaining high academic standards which promotes the analytical thinking and independent judgment among the prime stakeholders, enabling them to function responsibly in the globalized society.

Mission of the Institute

To be a world-class Institute, achieving excellence in teaching, research and consultancy in cutting-edge Technologies and be in the service of society in promoting continued education in Engineering, Technology and Management.

Quality Policy

To ensure high standards in imparting professional education by providing world-class infrastructure, top-quality-faculty and decent work culture to sculpt the students into Socially Responsible Professionals through creative team-work, innovation and research

Vision of the Department

Our vision is to develop the department into a full-fledged centre of learning in various fields of Electronics & Communication Engineering keeping in view the latest development.

Mission of the Department

The Mission of the department is to turn out full-fledged Engineers in the field of Electronics & Communication Engineering with an overall back-ground suitable for making a successful career either in industry/research or higher education in India and abroad. To inculcate professional behavior, strong ethical values, innovative research capabilities and leadership abilities in the young minds so as to work with a commitment to the progress of the nation.

Program Educational Objectives (B.Tech. – ECE)

Graduates will be able to

PEO 1	**:**	Excel in professional career & higher education, by acquiring knowledge in related fields of Electronics & Communication Engineering.
PEO 2	**:**	Exhibit leadership in their profession, through technological ability and contemporary knowledge for solving real life problems appropriately that are technically sound, economically feasible & socially acceptable.
PEO 3	**:**	Adapt to the emerging technologies for sustenance by exhibiting professionalism, ethical attitude & communication skills in their relevant areas of interest by engaging in lifelong learning.

Program Outcomes (B.Tech. – ECE)

At the end of the Program, a graduate will have the ability to

PO 1	**:**	An ability to apply knowledge of mathematics, science, fundamentals of engineering to solve electronics and communication engineering problems.
PO 2	**:**	An ability to identify, formulate and analyze and solve complex electronics and communication Engineering using the first principles of mathematics and engineering sciences.
PO 3	**:**	An ability to develop solutions to electronics and communication systems to meet the specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.
PO 4	**:**	An ability to design and perform experiments of electronic circuits and systems, analyze and interpret data to provide valid conclusions.
PO 5	**:**	An ability to learn, select and apply appropriate techniques, resources and modern engineering tools including prediction and modelling, to complex electronics and communication systems.
PO 6	**:**	An ability to assess the knowledge of contemporary issues to the societal responsibilities relevant to the professional practice.
PO 7	**:**	An ability to understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate knowledge for the need of sustainable development.
PO 8	**:**	An ability to demonstrate the understanding of professional, ethical responsibilities and norms of engineering practice.
PO 9	**:**	An ability to function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
PO 10	**:**	An ability to communicate effectively with the engineering community and with society at large.
PO 11	**:**	An ability to demonstrate knowledge and understanding of engineering and management principles and apply these to manage projects.
PO 12	**:**	An ability to recognize the need for, and engage in lifelong learning in the broadest context of technological change.

COURSE OBJECTIVES

On completion of this Subject/Course the student shall be able to:

S.No	Objectives
1	Learn the concepts of Power Amplifiers.
2	To give understanding of tuned amplifier circuits
3	Understand various multivibrators using transistors and sweep circuits.

COURSE OUTCOMES

The expected outcomes of the Course/Subject are:

S.No	Outcomes
1.	Design the power amplifiers
2.	Design the tuned amplifiers and analyze is frequency response
3.	Design Multivibrators and sweep circuits for various applications.
4.	Utilize the concepts of synchronization, frequency division and sampling gates

Signature of faculty

Note: Please refer to Bloom's Taxonomy, to know the illustrative verbs that can be used to state the outcomes.

GUIDELINES TO STUDY THE COURSE / SUBJECT

Course Design and Delivery System (CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

- Understand the principles of Learning
- Understand the psychology of students
- Develop instructional objectives for a given topic
- Prepare course, unit and lesson plans
- Understand different methods of teaching and learning
- Use appropriate teaching and learning aids
- Plan and deliver lectures effectively
- Provide feedback to students using various methods of Assessments and tools of Evaluation
- Act as a guide, advisor, counselor, facilitator, motivator and not just as a teacher alone

Signature of HOD

Date:

Signature of faculty

Date:

COURSE SCHEDULE

The Schedule for the whole Course / Subject is:

S. No.	Description	Duration (Date)		Total No. of Periods
		From	To	
1.	**UNIT - I** Large Signal Amplifiers: Class A Power Amplifier- Series fed and Transformer coupled, Conversion Efficiency, Class B Power Amplifier- Push Pull and Complimentary Symmetry configurations, Conversion Efficiency, Principle of operation of Class AB and Class –C and D Amplifiers.	05.02.2024	26.02.2024	14
2.	**UNIT - II** Tuned Amplifiers: Introduction, single Tuned Amplifiers – Q-factor, frequency response, Double Tuned Amplifiers – Q-factor, frequency response, Concept of stagger tuning and synchronous tuning	27.02.2024	06.03.2024	8
3.	**UNIT - III** Multivibrators: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt triggerusing Transistors.	11.03.2024	15.04.2024	17
4.	**UNIT - IV** Time Base Generators: General features of a Time base Signal, Methods of Generating Time Base Waveform, concepts of Transistor Miller and Bootstrap Time Base Generator, Methods of Linearity improvement.	22.04.2024	01.05.2024	07
5.	**UNIT - V** Synchronization and Frequency Division: Pulse Synchronization of Relaxation Devices, Frequency division in Sweep Circuits, Stability of Relaxation Devices, Astable Relaxation Circuits, Monostable Relaxation Circuits, Synchronization of a Sweep Circuit with Symmetrical Signals, Sine wave frequency division with a Sweep Circuit, A Sinusoidal Divider using Regeneration and Modulation. Sampling Gates: Basic operating principles of Sampling Gates, Unidirectional and Bi-directional Sampling Gates, Four Diode Sampling Gate,	02.06.2024	12.06.2024	14

	Reduction of pedestal in Gate Circuits			

Total No. of Instructional periods available for the course: 62 Hours

SCHEDULE OF INSTRUCTIONS - COURSE PLAN

Unit No.	Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	1	05.02.2024	1	UNIT - I Large Signal Amplifiers:	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	2	06.02.2024 & 07.02.2024	2	Classification of large signal Amplifiers	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	3	08.02.2024 & 09.02.2024	2	Series fed Class A Power Amplifier , Conversion Efficiency	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	4	12.02.2024 & 13.02.2024	2	Transformer coupled Class A power Amplifier, Conversion Efficiency	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	5	14.02.2024	1	Class B Power Amplifier	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson,

						2009
	6	17.02.2024 & 19.02.2024	2	Push Pull class B power Amplifier, conversion efficiency	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	7	20.02.2024	1	Complimentary Symmetry configurations	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	8	22.02.2024	1	Principle of operation of Class AB Power Amplifier	1 1	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	9	24.02.2024	1	Principle of operation of Class –C Power Amplifier	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	10	26.02.2024	1	Principle of operation of D Amplifiers.	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009

2	1	27.02.2024 & 28.02.2024	2	**UNIT- II** Tuned Amplifiers: Introduction,	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	2	29.02.2024 02.03.2024	2	single Tuned Amplifiers – Q-factor, frequency response,	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	3	02.3.2024 & 04.03.2024	2	Double Tuned Amplifiers – Q-factor, frequency response,	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
	4	05.03.2024 & 06.03.2024	2	Concept of stagger tuning and synchronous tuning	2 2	Robert L. Boylestead, Louis Nashelsky - Electronic Devices and Circuits theory, 11th Ed.,Pearson, 2009
3	1	11.03.2024 & 12.03.2024	2	UNIT - III Multivibrators: Classification of Multivibrators	2 2	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	2	13.03.2024 & 14.03.2024	2	Analysis and Design of Fixed bias bistable Multivibrator	2 2	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital

						and Switching Waveforms – 2nd Ed., TMH, 2008
	3	15.03.2024 & 16.03.2024	2	Analysis and Design of self-bias bistable Multivibrator	2 2	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	4	18.03.2024	1	Commutating Capacitors, Collector Catching Diodes	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	5	19.03.2024	1	Triggering	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	6	21.03.2024	1	Analysis and Design of Monostable Multivibrator	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	7	26.03.2024	1	Calculation of Pulse width	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008

	8	28.03.2024 & 30.03.2024	2	Analysis and Design of Astable Multivibrator	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	9	08.03.2024 10.03.2024 & 15.03.2024	3	Analysis and Design of Schmitt Trigger	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
4	1	22.04.2023	1	UNIT - IV Time Base Generators:	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	2	24.03.2024	1	General features of a Time base Signal	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	3	25.04.2024	1	Methods of Generating Time Base Waveform	3 3	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	4	27.04.2024 & 29.24.2024	2	Concepts of Transistor Miller and Bootstrap Time Base Generator	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital

						and Switching Waveforms – 2nd Ed., TMH, 2008
	5	30.04.2024	1	Comparision of Time base genearators	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	6	01.05.2024	1	Methods of Linearity improvement.	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
5	1	02.05.2024	1	UNIT - V Synchronization and Frequency Division	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	2	04.05.2024	1	Pulse Synchronization of Relaxation Devices	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	3	06.05.2024 & 07.05.2024	1	Frequency division in Sweep Circuits, Stability of Relaxation Devices	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008

	4	08.05.2024 & 10.05.2024	1	Astable Relaxation Circuits, Monostable Relaxation Circuits,	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	5	03.06.2024 & 04.06.2024	2	Synchronization of a Sweep Circuit with Symmetrical Signals, Sine wave frequency division with a Sweep Circuit,	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	6	05.06.2024	1	A Sinusoidal Divider using Regeneration and Modulation.	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	7	06.06.2024	1	Sampling Gates: Basic operating principles of Sampling Gates	4 4	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	8	10.06.2024 & 11.06.2024	2	Unidirectional and Bi-directional Sampling Gates	5 5	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital and Switching Waveforms – 2nd Ed., TMH, 2008
	9	12.06.2024	2	Four Diode Sampling Gate, Reduction of pedestal in Gate Circuits	5 5	J. Millman, H. Taub and Mothiki S. PrakashRao - Pulse, Digital

						and Switching Waveforms – 2nd Ed., TMH, 2008

Signature of HOD

Date:

Signature of faculty

Date:

Note:
1. Ensure that all topics specified in the course are mentioned.
2. Additional topics covered, if any, may also be specified in bold.
3. Mention the corresponding course objective and outcome numbers against each topic.

LESSON PLAN (U-I)

Lesson No: 02, 03 Duration of Lesson: 1hr 40 min

Lesson Title: Classification of large signal Amplifiers

Instructional / Lesson Objectives:

- To make students understand Operating Point
- To identify Operating point on Dc load line
- To understand students the classification of Power amplifiers based on operating point

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 80 min for the lecture delivery 15 min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Explain Classification of Power Amplifiers

Signature of faculty

LESSON PLAN (U-II)

Lesson No: 01, 02 Duration of Lesson: 1hr 40min

Lesson Title: Tuned Amplifiers Classification

Instructional / Lesson Objectives:

- To make students understand tuned circuit
- To familiarize students on tuned circuits used in tuned amplifiers
- To understand students the concept of Quality factor

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10 min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Explain briefly about tuned amplifiers

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LESSON PLAN (U-III)

Lesson No: 04, 05 Duration of Lesson: 1hr 40min

Lesson Title: Triggering

Instructional / Lesson Objectives:

- To make students understand the Stable states
- To familiarize students on triggering
- To understand students on applying triggering

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:

(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Explain various types of triggering.

Refer assignment-III & tutorial-III sheets.

Signature of faculty

LESSON PLAN (U-IV)

Lesson No: 04, 05 Duration of Lesson: 1hr 40min

Lesson Title: Bootstrap & Miller time base generators

Instructional / Lesson Objectives:

- To make students understand the concept of. Sweep time
- To familiarize students on Sweep Circuits

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:

(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Explain Bootstrap and Miller time base generators.

Refer assignment-IV & tutorial-IV sheets.

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LESSON PLAN (U-V)

Lesson No: 11, 12 Duration of Lesson: 1hr 40min

Lesson Title: Sampling gates

Instructional / Lesson Objectives:

- To make students understand the concept of Sampling gate
- To familiarize students on types of Sampling gates

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:

(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Explain briefly about Sampling gates

Refer assignment-V& tutorial-V sheets.

Signature of faculty

ASSIGNMENT – 1

This Assignment corresponds to Unit No. 1

Question No.	Question	Objective No.	Outcome No.
1	Distinguish between small signal and large signal amplifiers. How are the power amplifiers classified? Describe their characteristics.	1	1
2	List out the advantages and disadvantages of All power Amplifiers?	1	1

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Date:

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Date:

ASSIGNMENT – 2

This Assignment corresponds to Unit No. 2

Question No.	Question	Objective No.	Outcome No.
1	Explain Single Tuned Amplifier with neat circuit diagram and derive the following a) Resonant frequency b) Quality Factor c)Voltage Gain d) Bandwidth	2	2
2	Explain Double Tuned Amplifier with neat circuit diagram and derive the following a) Resonant frequency b) Quality Factor c)Voltage Gain d) Bandwidth	2	2

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Date:

ASSIGNMENT – 3

This Assignment corresponds to Unit No. 3

Question No.	Question	Objective No.	Outcome No.
1	Explain design of fixed bias and self-bias Bistable multivibrator	3	3
2	Explain Monostable multivibrator with neat diagram and calculate pulse width.	3	3

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Date:

Signature of faculty

Date:

ASSIGNMENT – 4

This Assignment corresponds to Unit No. 4

Question No.	Question	Objective No.	Outcome No.
1	Define the terms slope error, displacement error and transmission error of time-base signal with the help of a neat circuit diagram and waveforms explain the working of a transistor Miller time base generator.	3	3
2	With the help of neat diagram explain the working of transistor Bootstrap time base generator.	3	3

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ASSIGNMENT – 5

This Assignment corresponds to Unit No. 5

Question No.	Question	Objective No.	Outcome No.
1	Distinguish between Synchronization and synchronization with frequency division?	3	4
2	Draw the circuit of two-diode bi-directional sampling gate. Explain its operation & derive expressions for gain and minimum control voltage in the circuit.	3	4

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Date:

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Date:

TUTORIAL – 1

This tutorial corresponds to Unit No. 1 (Objective Nos.: 1, Outcome Nos.: 1)

Q1. Audio Amplifiers ar

a) Class A
b) Class B
c) Class AB
d) NONE

Q2. What is the Maximum Efficiency in Class A Power Amplifier

a) 100%
b) 25%
c) 50%
d) 78.5%

Q3. Full form of Class D power Amplifier

a) Class Delay
b) Class Digital
c) Class Data
d) Class Decoder

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Date:

TUTORIAL – 2

This tutorial corresponds to Unit No. 2 (Objective Nos.: 2, Outcome Nos.: 2)

Q1. How many types of tuned amplifiers

a) 1
b) 2
c) 3
d) 4

Q2. **Which of the following type of frequencies does a tuned amplifier amplifies**

a) High Frequencies
b) Radio Frequencies
c) Low Frequencies
d) None

Q3. **Which of the following are the components of tuned amplifiers?**

a) Resistor
b) Inductor
c) Capacitor
d) All

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Date:

TUTORIAL SHEET – 3

This tutorial corresponds to Unit No. 3 (Objective Nos.: 3, Outcome Nos.: 3)

Q1. How many types of multivibrators

a) 1
b) 2
c) 3
d) 4

Q2 How man stable states in Astable Multivibrator

a) 1
b) 0
c) 2
d) 4

Q3. What is the pulse width of mono stable Multivibrator?

a) 1.1RC
b) 0.69RC
c) 1.38RC
d) 0.35RC

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Signature of faculty

Date:

TUTORIAL – 4

This tutorial corresponds to Unit No. 4 (Objective Nos.: 3, Outcome Nos.: 3)

Q1. In which circuit Positive ramp produced

a) Miller circuit
b) Bootstrap Circuit
c) Both
d) None

Q2. In which circuit hold time is zero

a) Miller Circuit
b) Bootstrap Circuit
c) Both
d) UJT

Q3. In which negative ramp produced2

a) Miller circuit
b) Bootstrap Circuit
c) Both
d) None

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Date:

TUTORIAL SHEET – 5

This tutorial corresponds to Unit No. 5 (Objective Nos.: 5, Outcome Nos.: 5)

Q1. In an ideal Sampling gate during Transmission

a) Vo=Vi b) Vo=1/ Vi c) Vo=Vi /2 d) None

Q2. Unidirectional gates transmit signals

a) Of only one Polarity
b) In only one direction
c) Of both the Polarities
d) None

Q3. Synchronization with symmetrical signals is possible for

a) Tp<=T0
b) Tp>=T0
c) Both
d) none

Signature of HOD Signature of faculty

Date: Date:

EVALUATION STRATEGY

Target (s)

a. Percentage of Pass : 95%

Assessment Method (s) (Maximum Marks for evaluation are defined in the Academic Regulations)

a. Daily Attendance
b. Assignments
c. Online Quiz (or) Seminars
d. Continuous Internal Assessment
e. Semester / End Examination

List out any new topic(s) or any innovation you would like to introduce in teaching the subjects in this semester

Case Study of any one existing application

Signature of HOD

Date:

Signature of faculty

Date:

COURSE COMPLETION STATUS

Actual Date of Completion & Remarks if any

Units	Remarks	Objective No. Achieved	Outcome No. Achieved
Unit 1	completed on 26.02.2024	1	1
Unit 2	completed on 06.03.2024	2	2
Unit 3	completed on 15.04.2024	3	3
Unit 4	completed on 01.05.2024	3	3
Unit 5	completed on 12.06.2024	3	4

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Date:

Signature of faculty

Date:

Mappings

1. **Course Objectives-Course Outcomes Relationship Matrix**
(Indicate the relationships by mark "X")

Course-Outcomes / Course-Objectives	1	2	3	4	5
1	H	M			
2		H			
3			H		
4				H	M
5				M	H

2. **Course Outcomes-Program Outcomes (POs) & PSOs Relationship Matrix**
(Indicate the relationships by mark "X")

CO's /PO's	PO 1	PO2	PO 3	PO 4	PO5	PO6	PO7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	L	-	H	M	-	-	-	-	L	H	L	L
CO2	H	H	H	L	-	M	M	-	-	-	-	L	H	M	L
CO3	H	H	H	L	-	M	M	-	-	-	-	L	H	L	L
CO4	H	H	H	L	-	H	M	-	-	-	-	L	L	M	L
CO5	H	H	H	L	-	M	M	-	-	-	-	L	L	L	L

3-HIGH **2-MEDIUM** **1-LOW**

Rubric for Evaluation

Performance Criteria	Unsatisfactory	Developing	Satisfactory	Exemplary
	1	2	3	4
Research & Gather Information	Does not collect any information that relates to the topic	Collects very little information some relates to the topic	Collects some basic Information most relates to the topic	Collects a great deal of Information all relates to the topic
Fulfill team role's duty	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.
Share Equally	Always relies on others to do the work.	Rarely does the assigned work - often needs reminding.	Usually does the assigned work - rarely needs reminding.	Always does the assigned work without having to be reminded
Listen to other team mates	Is always talking—never allows anyone else to speak.	Usually doing most of the talking-- rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.

II B.TECH IV SEMESTER I MID EXAMINATIONS - APRIL 2024

Branch: B.Tech(ECE) **Max. Marks: 30**

Date: 03-Apr-2024 FN **Time: 120 Minutes**

Subject: Electronic Circuit Analysis, EC405PC

PART-A

ANSWER ALL THE QUESTIONS **10X1M=10M**

Q.No	Question	CO	BTL
1.	What is the Maximum efficiency in Class A Power Amplifier ( ) (A). 100% (B). 50% (C). 25% (D).78.50%	CO1	1
2.	Class C Power Amplifier Other Name ( ) (A). Tuned Amplifier (B). RF Amplifier (C). Both a and b (D). None	CO1	1
3.	What is the disadvantage of transformer Coupled Class A Power Amplifiers ( ) (A). Less Efficiency (B). Bulky,Costlier (C). Less no. of Components (D). Efficiency is less compared to seried fed Class A	CO1	1
4.	Efficiency of Class D Power Amplifier (A). 25% (B). 50% (C). 78.50% (D). 100%	CO1	2
5.	LC circuit in a tuned amplifier is also called ( ) (A). Resonance Circuit (B). Tank circuit (C) Resistive Circuit (D) Both a and b	CO2	1
6.	Which of the following are the componenets of tuned amplifiers? ( ) (A). Inductor (B). Capacitor (C). Resistor (D). All of the above	CO2	1
7.	Which of the following is the formula of quality factor of tuned based amplifier ( ) (A). Inductor Impedance/ Resistance (B) Capacitor Impedance/Resistance (C). Resistor Impedance/Reactance (D). B.th a and b	CO2	2
8.	What is the formula for resonant frequency ( ) (A). 1/[2LC] (B). 1/2LC (C). 1/2ΠsqrtofLC (D). 1/[2ΠLC]	CO2	1
9.	How many types of multivibrator ( ) (A).1 (B).2 (C). 3 (D). 4	CO3	1
10.	How many stable states in Astable multivibrator ( ) (A). 0 (B). 1 (C).2 (D). 3	CO3	1

PART-B

ANSWER ANY FOUR **4X5M=20M**

Q.No	Question	CO	BTL
11.	Explain Class C Power Amplifier and derive efficiency	CO1	3
12.	Explain Complementary Symmetry Class B Power Amplifier with neat Waveforms	CO1	2
13.	Explain effect of bandwidth in cascading of single tuned amplifier	CO2	3
14.	Explain Double tuned Amplifier with neat diagram	CO2	3
15.	Explain analysis of fixed bias binary with circuit diagram	CO3	3
16.	Explain brief Classification of Multivibrators	CO3	2

II B.TECH IV SEMESTER II MID EXAMINATIONS - JUNE 2024

Branch : B.Tech. (ECE) **Max. Marks : 30M**
Date : 20-Jun-2024 Session : Morning **Time : 120 Min**
Subject : Electronic Circuit Analysis,EC405PC

PART - A

ANSWER ALL THE QUESTIONS **10 X 1M = 10M**

Q.No	Question		CO	BTL
1.	How many unstable states in Astable Multivibrator (A). 1 (B). 2 (C). 0 (D). None	( )	CO3	L1
2.	Which circuit is called as Square wave Converter (A). Bistable Multivibrator (B). Monostable Multivibrator (C). Astable Multivibrator (D). Schmitt trigger	( )	CO3	L1
3.	In Which circuit hold time is zero (A). Miller circuit (B). Bootstrap sweep circuit (C). UJT Relaxation circuit (D). None	( )	CO4	L1
4.	In which circuit Postive ramp produced (A). Miller circuit (B). Bootstrap sweep circuit (C). both (D). None	( )	CO4	L1
5.	Miller sweep generator produces (A). Postive going rump (B). Negative going ramp (C). constant (D). None	( )	CO4	L1
6.	In voltage time base gencarator (A). Voltage proportional to time (B). Current Proportional to time (C). Voltage proportional Current (D). None	( )	CO4	L1
7.	Synchronization with symmetrical signals is possible for (A). Tp<=T0 (B). Tp>=T0 (C). Both (D). None	( )	CO5	L1
8.	In an ideal Sampling gate during Transmission (A). Vo=Vi (B). Vo=1/Vi (C). Vo=Vi/2 (D). None of these	( )	CO5	L1
9.	Synchronization of a signal compared with (A). continuous Signal (B). square signal (C). Sawtooth signal (D). None	( )	CO5	L1
10.	Sampling gates are also called as (A). Logic Gates (B). Linear Gates (C). Both (D). None	( )	CO5	L1

PART - B

ANSWER ANY FOUR **4 X 5M = 20M**

Q.No	Question	CO	BTL
11.	Explain schmitt trigger with neat circuit diagram and waveforms	CO3	L2
12.	With the help of neat circuit diagram and waveforms, explain the working of a collector coupled Astable Multivibrator? Obtain the expression for frequency in Astable Multivibrator	CO3	L3
13.	Explain Bootstrap sweep generator with neat circuit diagram and waveforms	CO4	L3
14.	Explain Linearity Improvement	CO4	L2
15.	Explain the basic principles of sampling gates using series switch and also give the applications of sampling gate	CO5	L3
16.	With neat circuit diagram, waveforms explain the frequency division in monostable multivibrator	CO5	L2

ANURAG Engineering College

(An Autonomous Institution)

Ananthagiri (V & M), Suryapet (Dt.), Telangana - 508206.

Electronics & Communication Engineering - A

II B.Tech II Semester Mid Marks List

S.No.	H.T.No.	Name of the Student	Mid - I Marks (30)	Mid - II Marks (30)	Avg of Mid-I & Mid-II (A)	Assignment - I (5)	Assignment - II (5)	Avg of Assg.-I & Assg.-II (B)	Viva Voce (5) (C)	Total (A+B+C)
1	22C11A0401	VANKA ADARSH REDDY	16	16	16	5	5	5	5	26
2	22C11A0402	PILLALAMARRI AJAY	14	14	14	5	AB	3	5	22
3	22C11A0404	THUNKOJU AKHIL	30	27	29	5	5	5	5	39
4	22C11A0405	GADDAM AKHILA	15	29	22	5	5	5	5	32
5	22C11A0407	AITHAGANI ANUSHA	29	29	29	5	5	5	5	39
6	22C11A0408	KARISHA ASHOK	18	27	23	5	5	5	5	33
7	22C11A0409	KILARU BHASWANTH KUMAR	18	29	24	5	5	5	5	34
8	22C11A0410	ERLA BHAVANA	27	29	28	5	5	5	5	38
9	22C11A0411	BANOTHU CHANDRA SHEKAR	20	13	17	5	5	5	5	27
10	22C11A0413	GUGULOTHU DIVYA	30	30	30	5	5	5	5	40
11	22C11A0414	KOTHAPALLI DIVYA JYOTHI	22	27	25	5	5	5	5	35
12	22C11A0415	THALLA GAYATHRI	29	29	29	5	5	5	5	39
13	22C11A0416	GODHUMALA GOPICHAND	29	27	28	5	5	5	5	38
14	22C11A0417	BHUKYA HARSHITHA	26	30	28	5	5	5	5	38
15	22C11A0418	REDDYMALLA JANAKI RAM REDDY	11	8	10	5	5	5	5	20
16	22C11A0419	SHAIK JASMINE	27	29	28	5	5	5	5	38
17	22C11A0420	JANAPATI JYOSHNA	26	29	28	5	5	5	5	38
18	22C11A0421	DHARAVATH KARTHIK	16	24	20	5	5	5	5	30
19	22C11A0422	JONNALAGADDA KAVYA	22	29	26	5	5	5	5	36

20	22C11A0423	JONNALAGADDA KAVYA SREE	20	29	25	5	5	5	5	35
21	22C11A0424	SHAIK KHATIJA	30	30	30	5	5	5	5	40
22	22C11A0425	KONDRU LAKSHMI	AB	22	11	5	5	5	5	21
23	22C11A0426	BODA LIKHITHA	27	27	27	5	5	5	5	37
24	22C11A0427	KUNDURU LIKHITHA REDDY	26	28	27	5	5	5	5	37
25	22C11A0428	CHINTHAKUNTLA LOKESH REDDY	29	30	30	5	5	5	5	40
26	22C11A0429	KOLLURI MADHU	14	15	15	5	5	5	5	25
27	22C11A0430	GUJJULA MAMATHA	AB	AB	0	AB	AB	0	AB	0
28	22C11A0431	MADASU MAMATHA	AB	AB	0	AB	AB	0	AB	0
29	22C11A0432	CHINNAM MANASA	15	17	16	5	5	5	5	26
30	22C11A0433	NANNEBOINA MEGHANA	30	29	30	5	5	5	5	40
31	22C11A0434	BHUKYA MOKSHAGNA	26	25	26	5	5	5	5	36
32	22C11A0435	GUNDLA NANDINI	29	30	30	5	5	5	5	40
33	22C11A0436	AKULA NARESH	27	30	29	5	5	5	5	39
34	22C11A0437	KODI NAVEEN	19	27	23	5	5	5	5	33
35	22C11A0438	POLOJU NAVEEN	27	29	28	5	5	5	5	38
36	22C11A0439	VARRA NAVEEN REDDY	15	18	17	5	5	5	5	27
37	22C11A0440	MALLELA NAVYA	26	30	28	5	5	5	5	38
38	22C11A0441	PAGADALA NAVYA	30	30	30	5	5	5	5	40
39	22C11A0442	MADDURI NICHITHA	26	29	28	5	5	5	5	38
40	22C11A0443	KOVVURI NIKHIL	5	10	8	5	5	5	5	18
41	22C11A0444	GUDIPATI NIKHIL SAI KUMAR	16	29	23	5	5	5	5	33
42	22C11A0445	NAGIREDDY NIRANJAN REDDY	27	28	28	5	5	5	5	38
43	22C11A0446	ENUGURTHI NITHIN	18	16	17	5	5	5	5	27
44	22C11A0447	BANALA NITHIN	24	27	26	5	5	5	5	36

		VAMSHI								
45	22C11A0448	UDARI NITHISH KUMAR	18	20	19	5	5	5	5	29
46	22C11A0449	AKARAPU POOJITHA	29	30	30	5	5	5	5	40
47	22C11A0450	BOLLAKA POOJITHA	30	30	30	5	5	5	5	40
48	22C11A0451	YARAGANI PRAJVAL	21	25	23	5	5	5	5	33
49	22C11A0453	MAMIDI PRIYANKA	26	27	27	5	5	5	5	37
50	22C11A0454	THOKALA PURUSHOTHAM	15	17	16	5	5	5	AB	21
51	22C11A0455	MOHAMMAD RAFI	15	14	15	5	5	5	5	25
52	22C11A0456	NUKALA RAJAGOPAL REDDY	29	30	30	5	5	5	5	40
53	22C11A0457	K RAJU	29	30	30	5	5	5	5	40
54	22C11A0458	PANGOTH RAM KUMAR	22	27	25	5	5	5	5	35
55	22C11A0459	SHEELAM RAMAKANTH	16	25	21	5	5	5	5	31
56	22C11A0460	BANOTHU RAVI	28	30	29	5	5	5	5	39

ANURAG Engineering College

(An Autonomous Institution)

Ananthagiri (V & M), Suryapet (Dt.), Telangana - 508206.

Electronics & Communication Engineering - B

II B.Tech II Semester Mid Marks List

S.No.	H.T.No.	Name of the Student	Mid - I Marks (30)	Mid - II Marks (30)	Avg of Mid -I & Mid -II (A)	Assignment - I (5)	Assignment - II (5)	Avg of Assg. -I & Assg. -II (B)	Viva Voce (5) (C)	Total (A+B+C)
1	22C11A0461	KOTIKA RAVI KIRAN	28	30	29	5	5	5	5	39
2	22C11A0462	SHAIK RESHMA	24	30	27	5	5	5	5	37
3	22C11A0463	BADETI SAI	27	26	27	5	5	5	5	37
4	22C11A0464	SAMPATHARAO SAI KUMAR	21	30	26	5	5	5	5	36
5	22C11A0465	KALLA SAI MANOJKUMAR	28	26	27	5	5	5	5	37
6	22C11A0466	KANDULA SAIKIRAN	16	24	20	5	5	5	5	30
7	22C11A0467	SHAIK SAMEER	27	23	25	5	5	5	5	35

8	22C11A0469	ANANTHARAPU SANJAN	25	24	25	5	5	5	5	35
9	22C11A0470	PALLY SANTHOSH REDDY	20	20	20	5	5	5	5	30
10	22C11A0471	SHAIK SHAFIQ	26	30	28	5	5	5	5	38
11	22C11A0472	N SHARATH CHANDRA	30	30	30	5	5	5	5	40
12	22C11A0473	BATTULA SHARATH GOPAL	14	18	16	5	5	5	5	26
13	22C11A0474	KUMBHAM SHIRISHA	20	22	21	5	5	5	5	31
14	22C11A0475	PANUGOTH SHIVA	25	24	25	5	5	5	5	35
15	22C11A0476	BOLISETTY SHIVA SHANKAR	14	22	18	5	5	5	5	28
16	22C11A0477	CHENNAKESHAV A SHREYA	27	25	26	5	5	5	5	36
17	22C11A0478	BHUKYA SIDDU NAIK	17	30	24	5	5	5	5	34
18	22C11A0479	MEKALA SINDHU	30	30	30	5	5	5	5	40
19	22C11A0480	LAVORI SRAVANI	30	30	30	5	5	5	5	40
20	22C11A0481	LINGAM SRAVANI	21	30	26	5	5	5	5	36
21	22C11A0482	BODDU SREEJA	23	29	26	5	5	5	5	36
22	22C11A0483	EATUKURI SRI LAKSHMI	30	30	30	5	5	5	5	40
23	22C11A0484	KAVURI SRICHANDANA	24	29	27	5	5	5	5	37
24	22C11A0485	KUKKALA SRUJAN	15	25	20	5	5	5	5	30
25	22C11A0486	RAVELLA SURYA	19	22	21	5	5	5	5	31
26	22C11A0487	KUNCHALA TRIVENI	29	30	30	5	5	5	5	40
27	22C11A0488	PEDANATI UDAY SAINADH	AB	AB	0	5	AB	3	AB	3
28	22C11A0489	SIRAM SETTI UMAMAHESH	29	29	29	5	5	5	5	39
29	22C11A0490	BANOTHU USHA	27	30	29	5	5	5	5	39
30	22C11A0491	DHANIYAKULA USHASRI	22	30	26	5	5	5	5	36
31	22C11A0492	ATHKURI VAMSHI	25	29	27	5	5	5	5	37
32	22C11A0493	THAMMINENI VENNELA	13	19	16	5	5	5	5	26
33	22C11A0494	PALLA VIJAY KUMAR	AB	AB	0	AB	AB	0	AB	0
34	22C11A0495	GUNNAM VIJAY SIMHA REDDY	13	22	18	5	5	5	5	28
35	22C11A0496	KASANI VINAY TEJA	23	28	26	5	5	5	5	36
36	22C11A0497	TELAGORLA VINAY	22	28	25	5	5	5	5	35
37	22C11A0498	DAMMALAPATI VINOD KUMAR	19	30	25	5	5	5	5	35
38	22C11A0499	KATIKAM VISHVA TEJA	11	10	11	5	5	5	5	21
39	22C11A04A0	BANOTHU YAMINI NAIK	23	29	26	5	5	5	5	36
40	22C11A04A1	BASANAKARRA YASHWANTH	29	28	29	5	5	5	5	39

41	22C11A04A2	REMIDALA YASHWANTH	14	23	19	5	5	5	5	29
42	22C11A04A3	SAYYAD YASIN	15	22	19	5	5	5	5	29
43	22C11A04A4	MACHIREDDY PRATHYUSHA	25	28	27	5	5	5	5	37
44	22C11A04A5	REDDIMALLA BHANU PRAKASH	24	29	27	5	5	5	5	37
45	23C15A0401	AKHILESHWARI SUDDALA	14	23	19	5	5	5	5	29
46	23C15A0402	ANJALI CHILAKAMARRI	26	25	26	5	5	5	5	36
47	23C15A0403	DURGA SAI ACHANTA	24	25	25	5	5	5	5	35
48	23C15A0404	HARINI SHANAGAPATI	22	20	21	5	5	5	5	31
49	23C15A0405	LAXMI GAYATHRI NERELLA	27	26	27	5	5	5	5	37
50	23C15A0406	MUKESH SIVAKAVI	10	23	17	5	5	5	5	27
51	23C15A0407	NAVYA SRI MADURI	28	28	28	5	5	5	5	38
52	23C15A0408	RAMARAO THODETI	18	25	22	5	5	5	5	32
53	23C15A0409	SAMAD SHAIK	27	28	28	5	5	5	5	38
54	23C15A0410	SANDEEP ATHMAKURU	28	29	29	5	5	5	5	39
55	23C15A0411	VENKATA KRISHNA KARAMSETTI	26	25	26	5	5	5	5	36

ANURAG ENGINEERING COLLEGE

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(Approved by AICTE, New Delhi, Affiliated to JNTUH, Hyderabad, Accredited by NAAC with A+ Grade)

Ananthagiri (V & M), Kodad, Suryapet (Dist), Telangana.

Program			YEAR	SEMESTER	MID EXAMINATION
B.Tech. ✓	M.Tech.	M.B.A.	II	II	II

Regulation: R-22 | Branch or Specialization: ECE

HALL TICKET NO.: 2 2 C 1 1 A 0 4 7 2

Signature of Student: N Bharath Chandra

Course: Electronic Circuit Analysis

Signature of Invigilator with date: 20/06/24

Q.No. and Marks Awarded

1	2	3	4	5	6	7	8	9	10	11

Signature of the Evaluator:

Maximum Marks: 30 | Marks Obtained: 30

(Start Writing From Here)

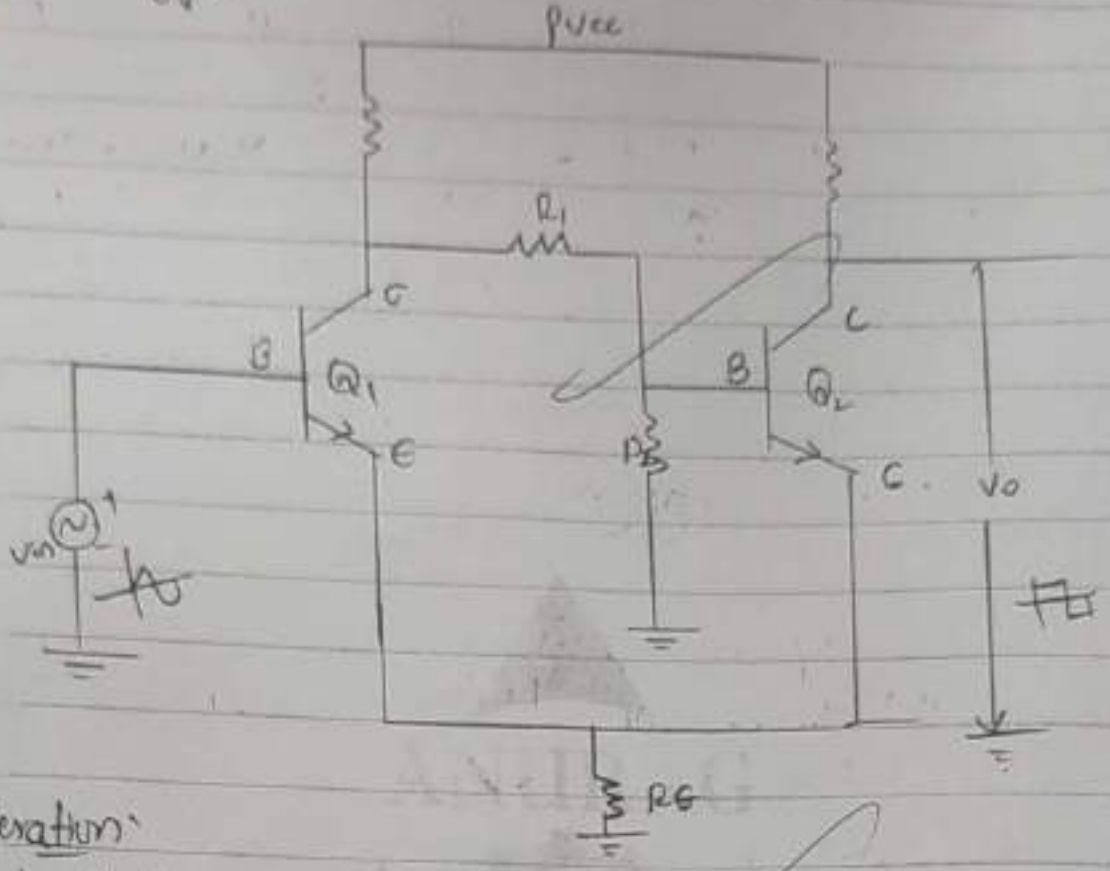
PART-A

1. B ✓
2. D ✓
3. C ✓
4. B ✓
5. B ✓
6. A ✓
7. C ✓
8. A ✓
9. C ✓
10. B ✓

X

PART-B

11 Schmitt trigger :-

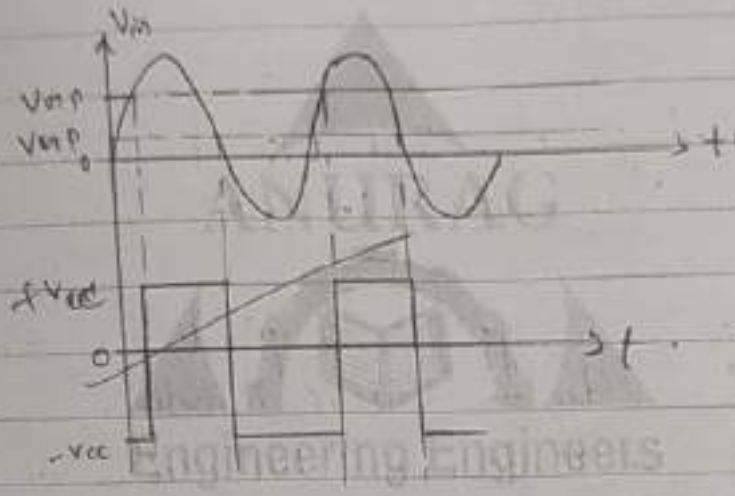


Operation:

* Schmitt trigger is also known as Emitter Coupled Bistable Multivibrator because the transistor Q_1 & Q_2 are coupled with emitter resistance (R_E). So, it is also called as Emitter Coupled Bistable Multivibrator.
* In this the input voltage is applied to the Q_1 Transistor and Output is observed at Q_2 transistor with respect to ground.
* In this Circuit, the Transistor Q_1 acts as in active region and Q_2 Transistor acts in Saturation region.
* Whenever the base voltage is less than the Cut-off voltage then the Transistor Q_1 & Q_2 are in Cut-off region.

* In this Circuit, the Circuit is operated in 3 different regions (active, Saturation, Cut off) so it is called as a Special type of Multivibrator
* In this, without any triggering the States are Transition from one State to other state
* If we give any i/p (square, Triangular or Sinusoida)) we get o/p as a Square wave so, it is also known as Square wave Converter
* It has two triggering points known as Opper Triggering point & Lower triggering point

Waveforms:-

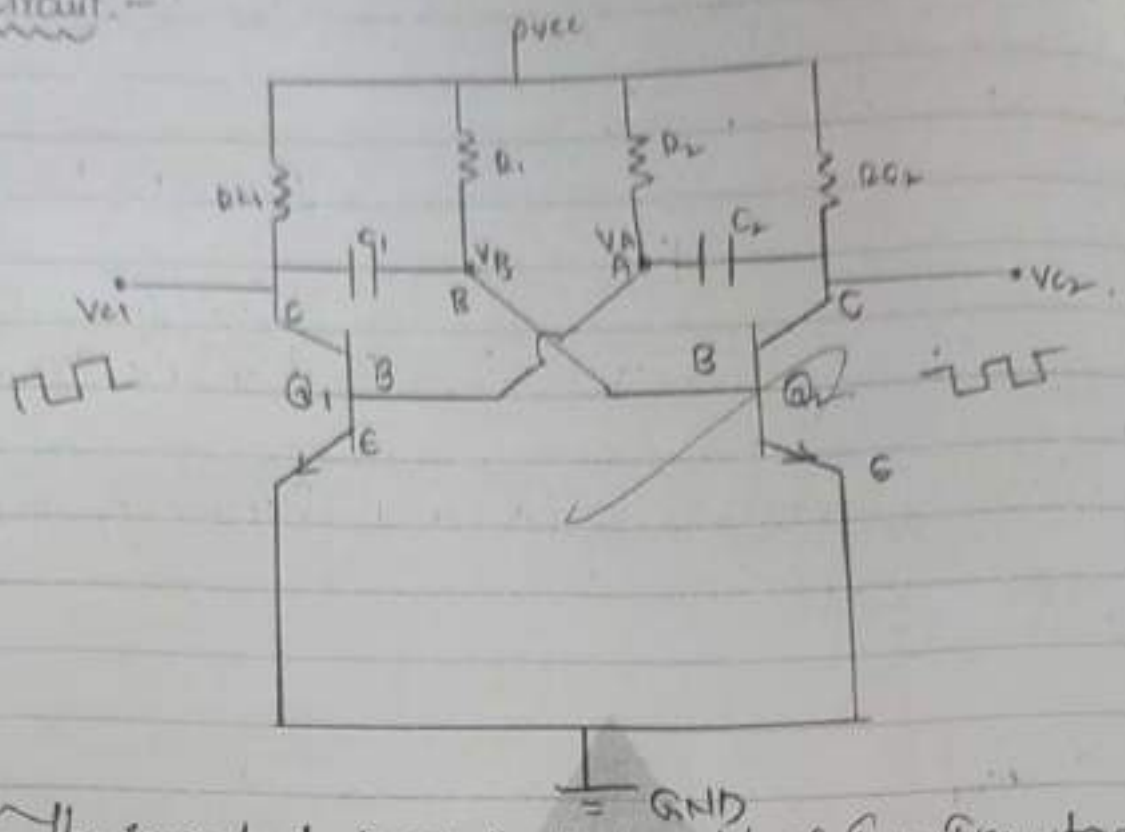


2. Collector Coupled Astable Multivibrator:

The Multivibrator which has no stable States and having two Quasi or Unstable States is known as Astable Multivibrator

* No External triggering is required to Change One State to another State
* It is also known as Free running Multivibrator because for each time division the pulse switch off or ON.
* Two Capacitors are used as the Coupling Capacitors in the Astable Multivibrator

Circuit:-



The important point is that o/p's of Two Transistor are always Complementary in astable Multi.

Operation:

Firstly Vcc supply is applied to both Transistor through R_1 & R_2, due to initial imbalance in the Circuit though the resistors are identical Only one of the Transistor will be ON and other is in OFF state.

Let Us Consider,

Case-1:- Q_2 is ON & Q_1 is in OFF.

i) Whenever the Transistor is Q_2 in ON state then the Capacitor C_2 which is earlier in Charging State will be discharges through $R_2 - C_2 - Q_{ON}$ at node A.

ii) The Capacitor C_1 will be Charges through $R_{C_1} - C_1 - Q_2 - ON$ at node B.

iii) Whenever C_2 discharges at some time the

Case-2: Q_1 ON & Q_2 is OFF.

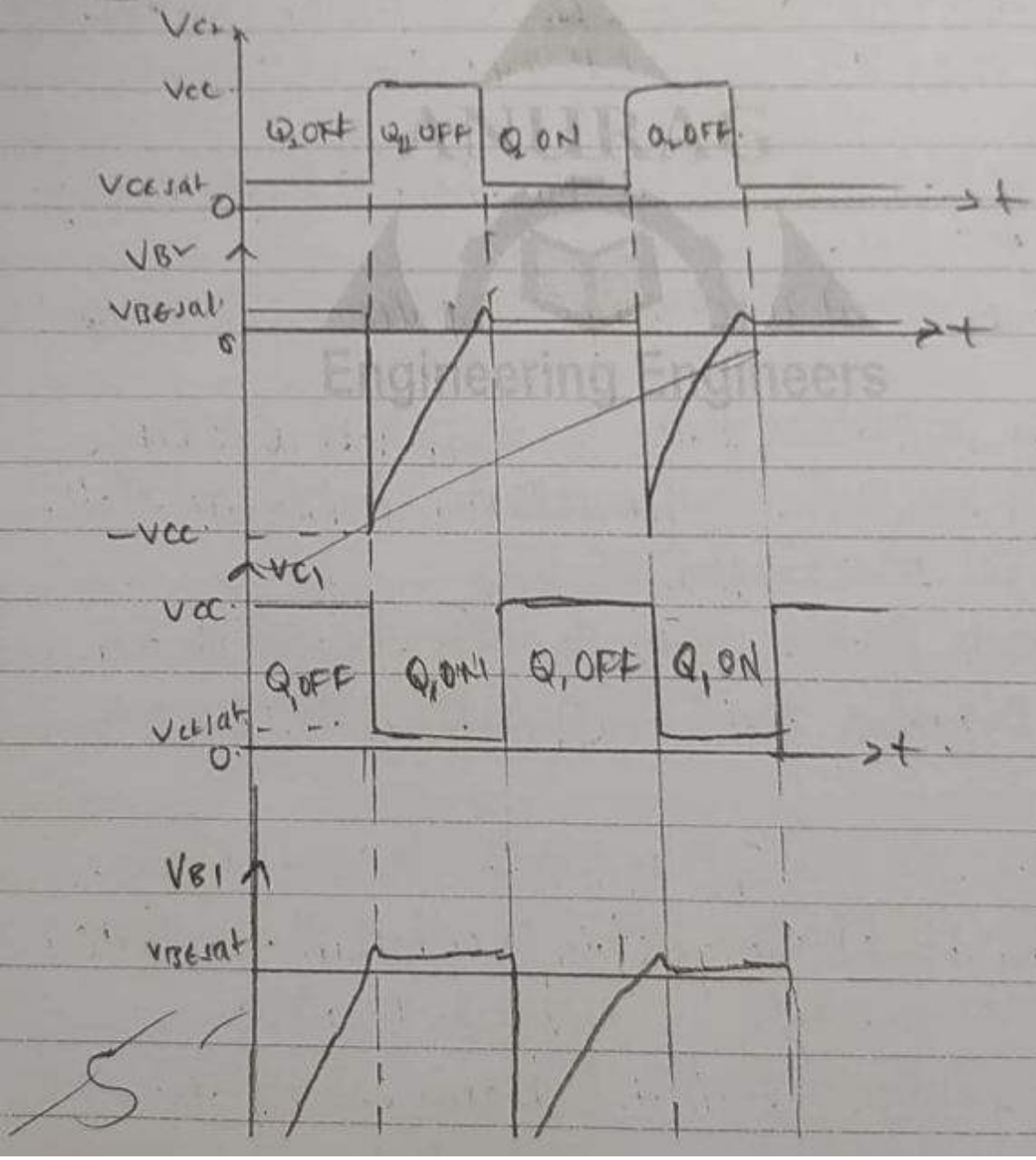
i) Whenever Q_1 is in ON. then C_1 discharges through $R_1 - C_1$ & Q_{ON} then it discharges through at node B.

ii) And simultaneously Capacitor C_2 charges through $R_{C_2} - Q_2$ & Q_{ON}.

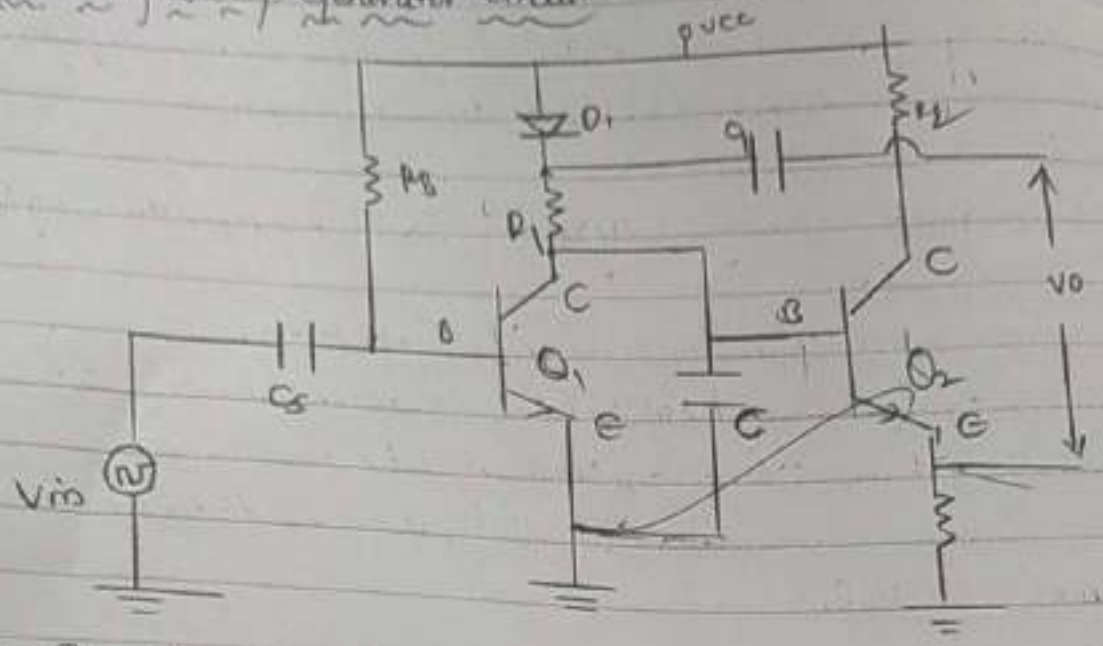
iii) At some time, the discharged Capacitor C_1 it will get small and small until the cut off voltage of Q_2 then it is on & Q_1 will be OFF.

iv) In this Cases, we understand that the Astable is free running Multi.

Waveforms:



13. Bootstrap Sweep Generator Circuit



* In this Transistor Q_1 & Q_2 will produce a time base signal. It is one of the applications of time base generator.
* The Capacitor which is at the base of Q_2 will give us sweep signal.
* The Input signal is always a pulse or a rectangular signal.
* In this the important thing is Q_1 acts a switch and Q_2 acts as an Emitter follower because the O/p is seen at the Emitter of Q_2.
* If the pulse is positive then Q_1 acts as ON switch
* If pulse is Negative then Q_1 acts as OFF switch

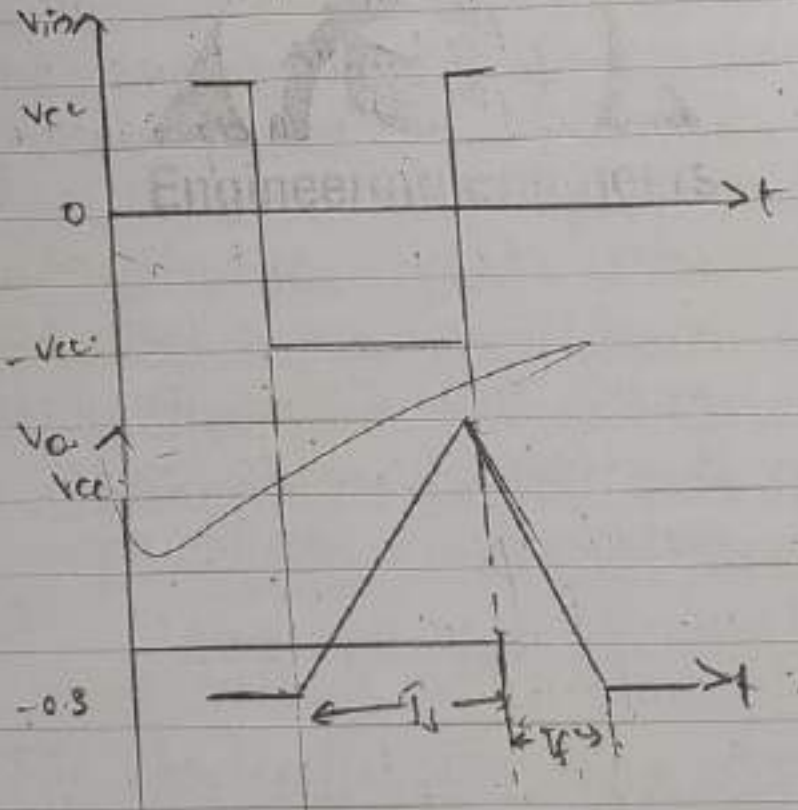
Operation:

Consider a 'Q_1' Transistor is in ON state then the Capacitor (C) Charges upto Vcc. then the Output of the first transistor which is observed as 0.3 V at V_{C_1} then it Connects to the base of Q_2 then ...

Consider a Negative pulse or polarity is applied to the base of Q_1 then the transistor will be in OFF and the Capacitor C, Charges Capacitor sweep through R_1 as the Capacitor C is very larger than sweep Capacitor the C Capacitor act a battery voltage then it gives supply to diode then diode is reverse biased and voltage drop across R_1 is constant and Capacitor Charges more and signal increases linearly as a positive ramp. Then automatically C is connected to Q_2 transistor then Q_2 will be in ON and whenever Negative pulse is removed the Capacitor discharges slowly

* Et is the Operation of bootstrap to generate time base signals.

Waveform:

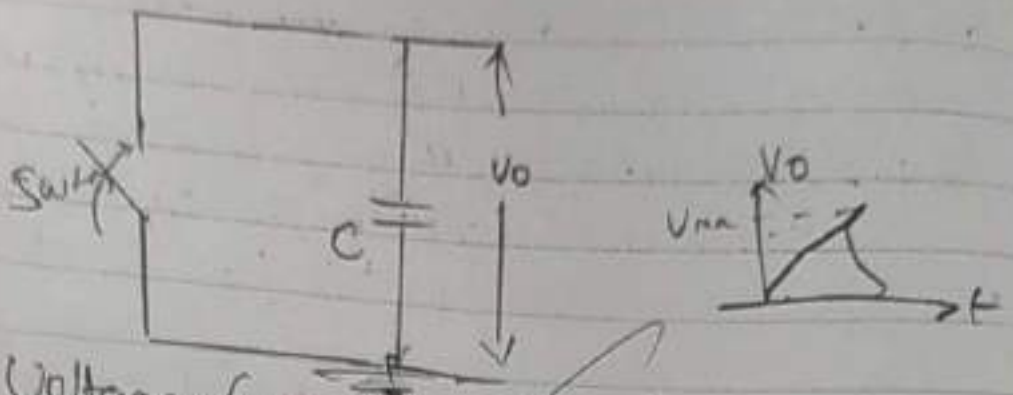


Linearity movement / Improvement

Linearity movement describes the signal improvement of linearity.

There it has two circuits in Linearity Improvement.

1. Voltage sweep circuit / Voltage time generator:-



In the voltage sweep circuit the sweep signal is produced with respect to capacitor and it is operated using switch

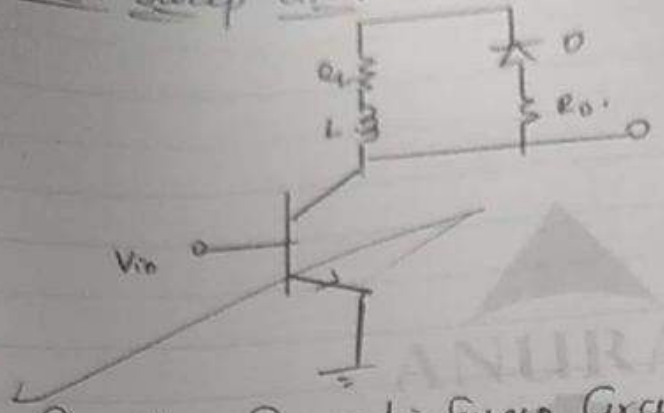
* Whenever the switch is in open circuit or OFF then the capacitor starts charging from initial to peak value say Vcc then the sweep signal is produced as capacitor starts charging from 0 to Vcc.
* Whenever the switch is short circuit or ON then the capacitor which stored is discharged slowly with respect to ground then the sweep voltage decreased
* In this voltage sweep generator the voltage is directly proportional to time.

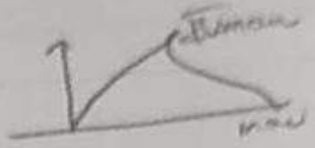
$V_o = \frac{1}{C}\int i\,dt$ by applying KVL

$= \frac{1}{C}\cdot\frac{V_s}{R} = \frac{V_s}{CR} = \frac{1}{C}\cdot\frac{V_s}{R}$ $\boxed{I = \frac{V}{R}}$

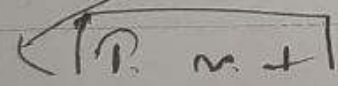
$\boxed{V_o \propto t}$

Current Sweep Circuit





* In this Current Sweep Circuit, the output is produced as Current waveforms then it Uses a passive element in the Circuit like RLC.
* But it Uses inductor used in the Circuit
* The inductor plays an important role in Calculating the sweep Current.
* The inductor does not change Current instantaneously
* If the input voltage is greater than V_r (Cut in voltage) then the ~~Capacitor~~ inductor starts increasing from 0 to max Current.
~~No Current.~~
* If the input voltage is smaller than Cut-in voltage then Current starts decreasing from max to min.
* In this Current is proportional to time.



ANURAG ENGINEERING COLLEGE

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Ananthagiri (V & M), Kodad, Suryapet (Dist), Telangana.

Program			YEAR	SEMESTER	MID EXAMINATION
B.Tech. ✓	M.Tech.	M.B.A.	II	II	I

HALL TICKET NO.

2	2	C	1	1	A	0	4	4	3

Regulation : R-22 Branch or Specialization: ECE

Course: Electronic Circuit Analysis

Signature of Student:

Signature of Invigilator with date:

Signature of the Evaluator:

Q.No. and Marks Awarded										
1	2	3	4	5	6	7	8	9	10	11

Maximum Marks: 30 Marks Obtained: 5.

(Start Writing From Here)

PART-A

1. D ✗
2. C ✓
3. B ✓
4. B ✗
5. B ✗
6. D ✓
7. A ✗
8. B ✗
9. C ✓
10. B ✗

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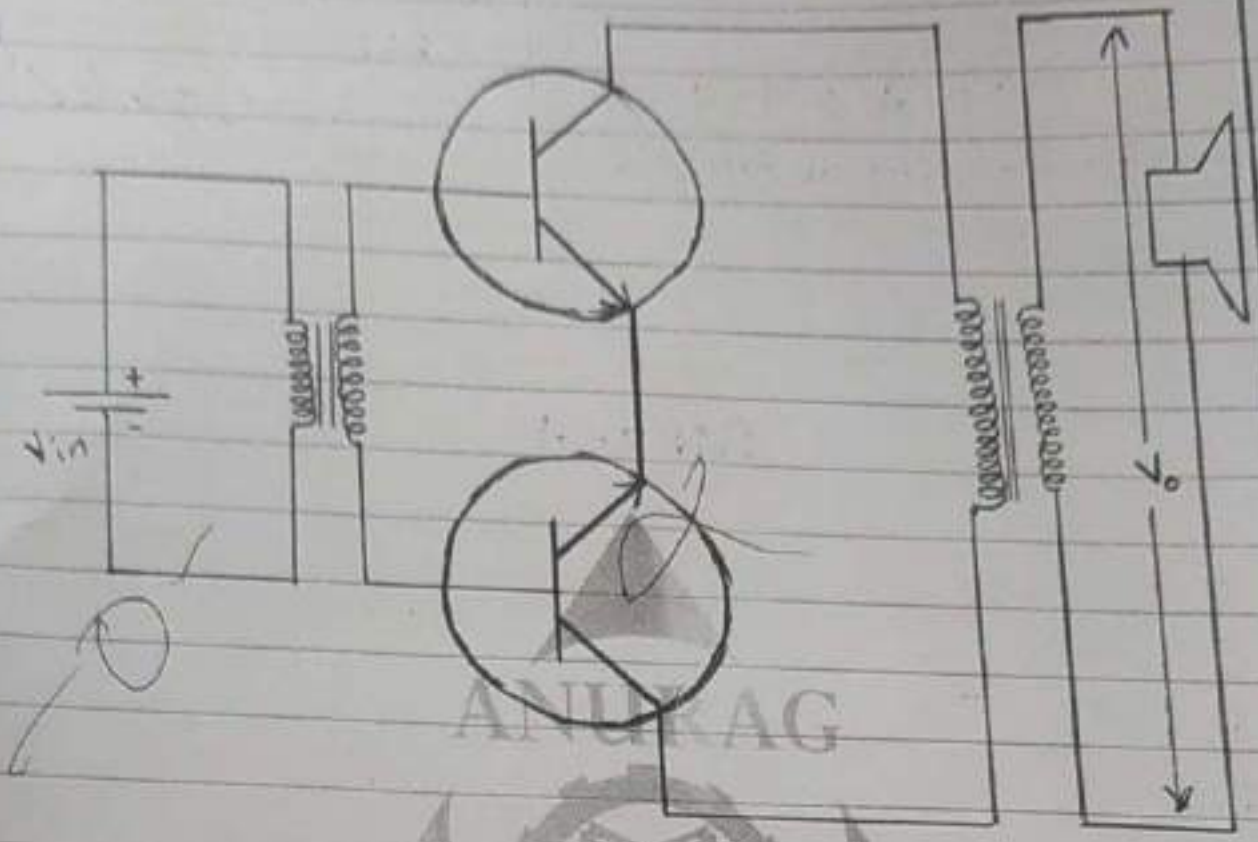
Part - B

12.



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Engineering Engineers

11. efficiency (η) = $\frac{P_{ac}}{P_{dc}} \times 100\ \%$ —(1)

AC power (P_{ac}) :-

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Program		
✓ B.Tech.	M.Tech.	M.B.A.

YEAR	SEMESTER	MID EXAMINATION
II	II	II

HALL TICKET NO.

2	2	C	1	1	A	0	4	1	8

Regulation: R-22 Branch or Specialization: ECE

Course: Electronic circuit analysis

Signature of Student: R. Jaraki varn

Signature of Invigilator with date: Lathender

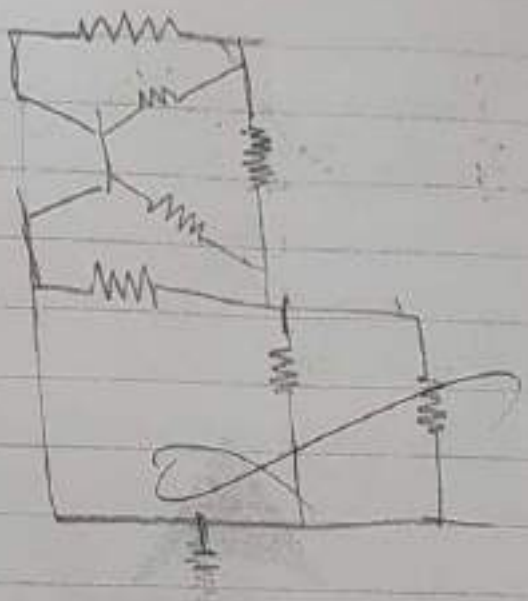
Signature of the Evaluator:

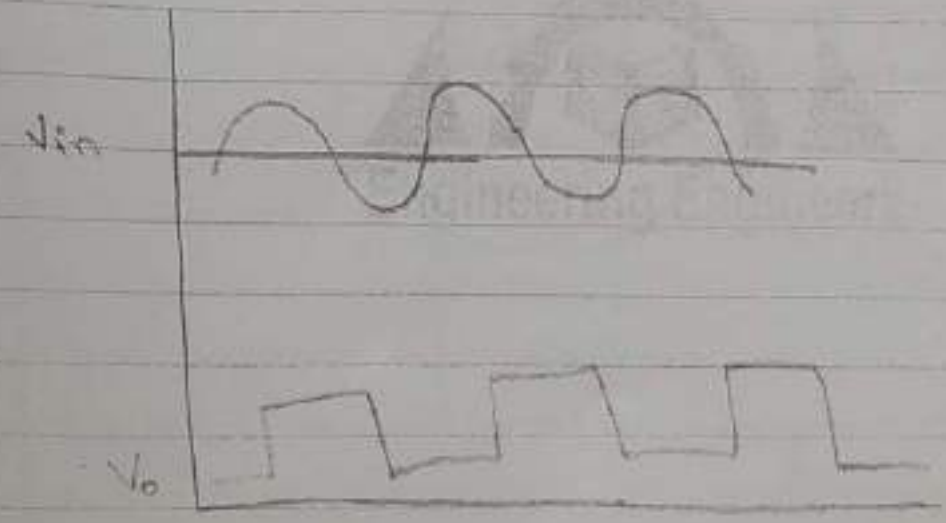
Q.No. and Marks Awarded										
1	2	3	4	5	6	7	8	9	10	11

Maximum Marks: 30 Marks Obtained: 8

(Start Writing From Here)

1) Schmitt trigger





V_i = V_{IH} Small

V_i = 0

Q_1 = OFF

Q_2 = Cannot of active Region

V_E = Potential RE

$V_E = I_{E_2} R_E$

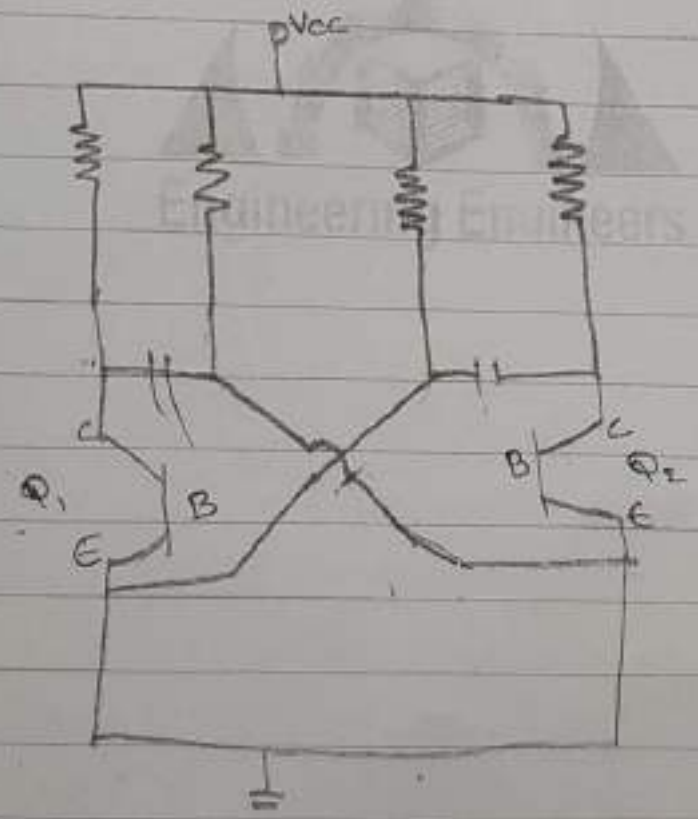
$I_E = I_B + I_C$

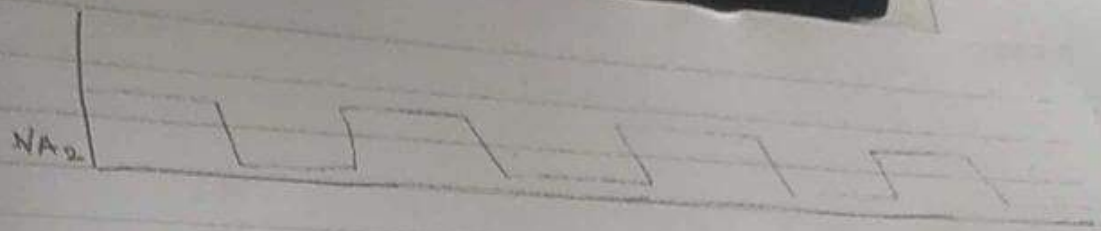
$I_{E_2} \simeq I_{E_2} R_E$

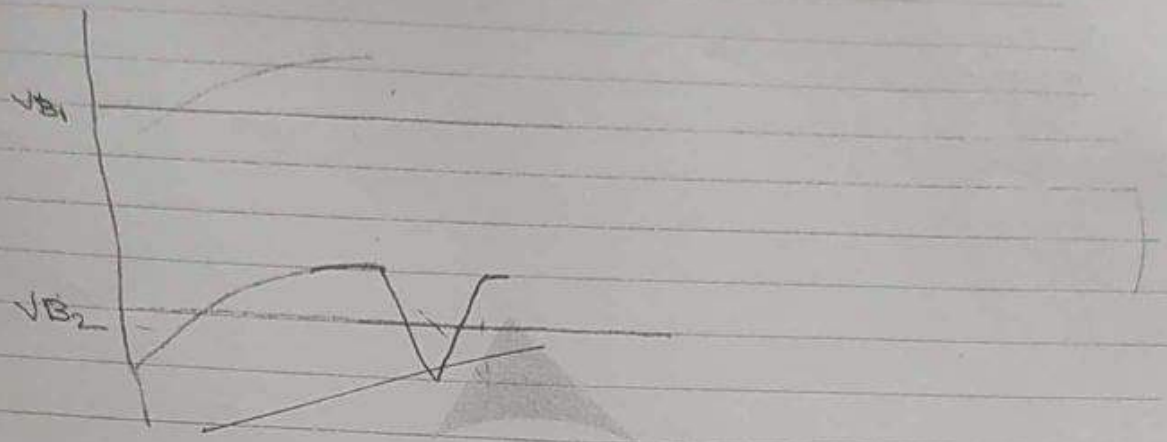
V_E =

Q_1 = ON , Q_2 = OFF

12) Astable multivibrator







$$T = T_1 \times T_2$$

$$Q = \frac{V_{A_1} \times V_{B_1}}{V_{A_2} \times V_{B_2}}$$

$$T = Q_1 \times Q_2$$

3

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(4)

1. Distinguish between synchronization and synchronization with frequency devision?

Ans- Synchronization and frequency division:—

⇒ In a pulse or digital system employs several different types of basic waveform generator like multivibrators, sweep generators blocking oscillators etc., as these are required for its subsystems.

⇒ It is very essential that these generators operate in synchronision i.e, in step with are another.

⇒ The frequencies of the waveforms may be Equal or different

⇒ If the frequencies are Equal there is no serials problem Encounters in running the generators synchronously.

⇒ However if the frequency of the waveform are not the same steps must be taken to ensure that the generator still run synchronously.

⇒ When generator with frequencies run in synchronization the synchronization is achived with different frequencies as for example one frequency being twice the other.

principle of synchronization:—

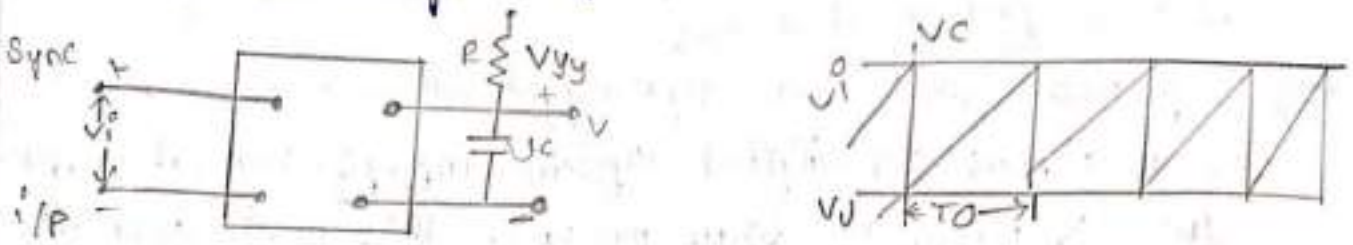
⇒ Let a unijunction transistor (UJT) relaxation oscillator be considered.

⇒ UJT is a current controlled negative resistance device which can be used as a switch.

⇒ It generates a voltage whose waveform is sawtooth signal

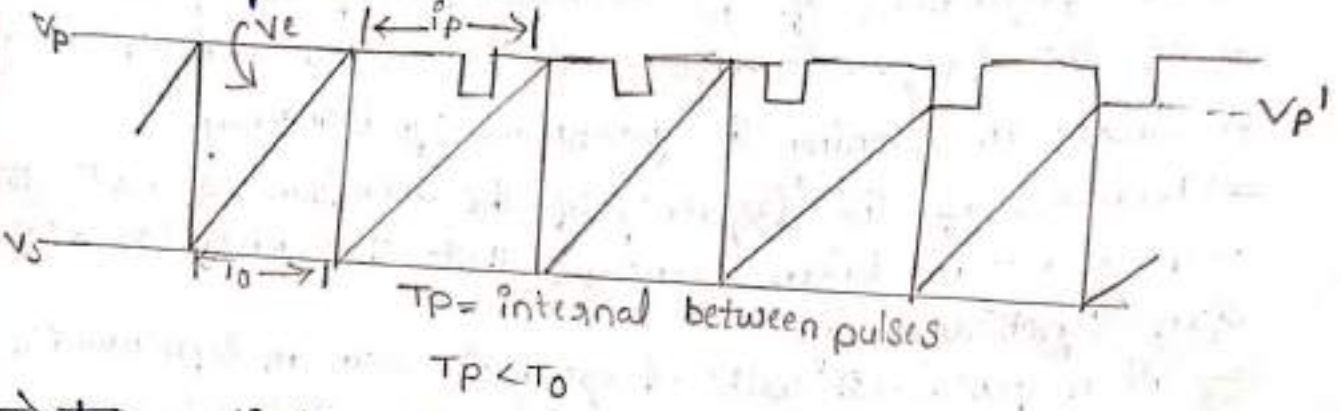
⇒ the voltage rises exponentially as the capacitor charges with UJT off, until it becomes Equal to the peak voltage Vp.

⇒ When the capacitor voltage Equal V_p the UJT becomes ON and the capacitor discharges. The voltage falls to the value V_v, the valley voltage.



⇒ from the circuit before the eapplications of the synchronising pulses at the sync input terminals of the device.

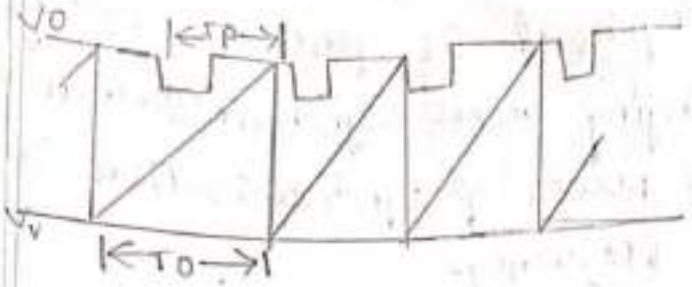
⇒ the situation which obtains after the application of the synchronising pulses.



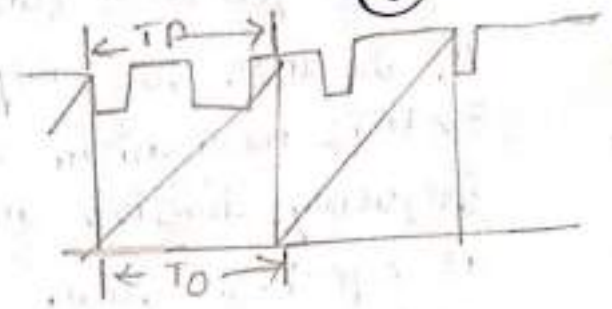
⇒ the application of synchronising pulses, in general, has the effect of lowering the peak voltage vp. Thus in the figure $V_p < V_p$.

⇒ It is seen that the first few pulses have no effect whatever on the operation of the generator and the generator continues to run unsynchronised, since these pulses fail to terminate the cycle pumatively because of their in adequate amplitude.

⇒ the generator now runs synchronisatiously with the synchronising pulses.



Tp > To



Tp < To
but every small pulse amplitude

Synchronization with Frequency Divisions:—

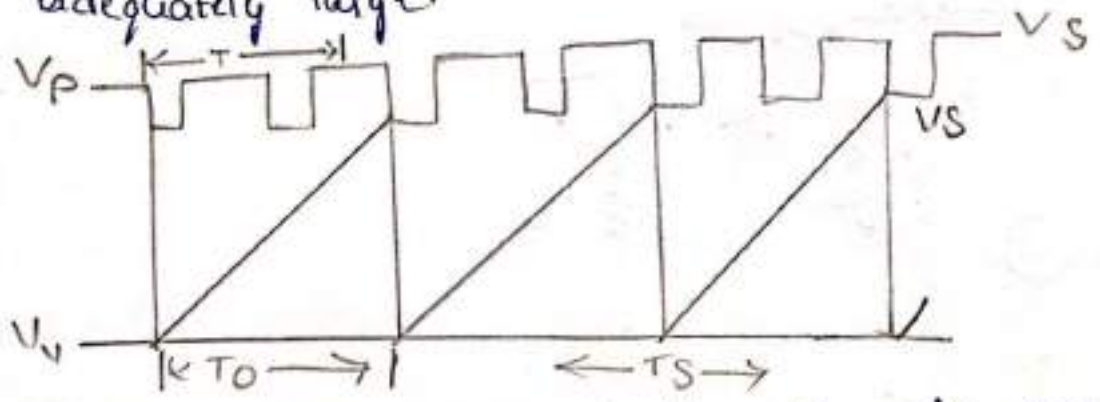
⇒ In 1:1 Synchronisation in which, after synchronism is reached, each succeeding pulse terminates the cycle permanetly

⇒ the conditions necessary to be fulfilled are two fold.

i, Tp must be less than To and

ii, the pulse amplitude must be adequately large so that it is capable capable of terminating the cycle permanetelly neay the peak.

⇒ Let us consider the situation when To is much larger than Tp, as for Example. To > 2Tp and the pulse amplitude is adequately large.



⇒ Also the sweep voltage is found to make one cycle for every two cycles of the synchronising pulses.

⇒ After Synchronism has been Established The of period of the generator decreases slightly i.e, Ts < To

⇒ the generator functions as a divider with a division factor of 2. since for every two cycles of the generator voltage.
⇒ this mechanism of bringing about synchronisation of frequency division and the power of synchronisation turned as synchronisation with frequency.
⇒ In the Example considered above

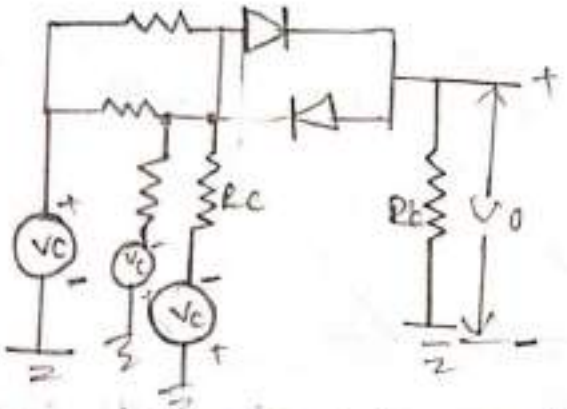
$T_0 > 2T_p$ with the result that $T_S = 2T_p = \frac{T_S}{T_P} = 2$

⇒ If $T_0 > 3T_p \Rightarrow T_0/T_p = 3$

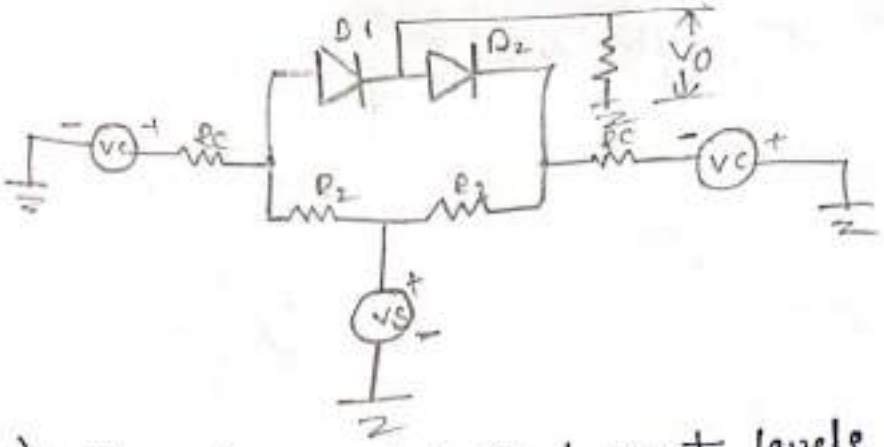
⇒ In such a circuit, for every n cycles of the synchronising pulses, the generator voltage would complete one cycle.

2. Draw the circuit of two-diode bi-directional sampling gate. Explain its operation & derive expressions. For gain and minimum control voltage in the circuit.

Bidirectional diode sampling gate:- Bidirectional sampling gate using diodes have basic advantages of linearity of operation. Also they can be adjusted easily to obtain zero pedestal.

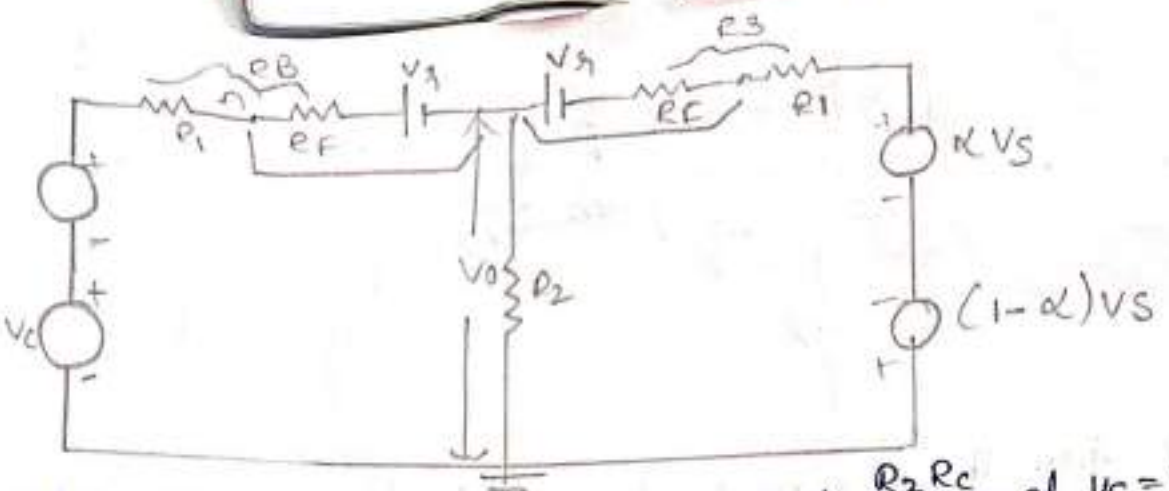


⇒ In this circuit two symmetrical gating voltages +ve & -ve are required the circuit redrawn as below.



⇒ When the control signal are at levels +ve & −ve respectively
⇒ when the sig of A is +ve & at B is −ve both diode D_1 & D_2 are ON and then a sample of Vs appears of the o/p.
⇒ If the diodes are identical in characteristics because of symmetry in the circuit of pedestal can appear at the o/p.
i) When $V_c(D_1) = +ve$ & $V_c(D_2) = -Vc$ Then D_1 & D_2 are forward biased is closed switches $V_o = V_s$. At this period time is called transmission period.
⇒ At this condition $V_s = 0V$ means $V_o = 0V$ based on control signal circuit acts as NAND gate operation with Vc = logic '1' & −ve = logic '0' the o/p is zero pedestal.
⇒ V_o is only function of V_s when D_1 & D_2 consists voltage of Vc & −Vc.
ii) When $V_c(D_1) = -V_A$ & $V_c(D_2) = +V_A$ D_1 & D_2 are reverse biased and acts as open circuit $V_o = 0$ V_o is independent of V_s. This period is called non transmission period.

Gain − 1) Gain $A = \frac{V_o}{V_s}$ and calculate V_c min
⇒ At transmission period D_1 & D_2 are forward biased V_c min = V_c (min +ve to be applied D_1)
⇒ At non transmission period D_1 & D_2 are reverse biased V_o min = V_o min (min +ve voltage to be applicate D_2)
⇒ At circuit can be redrawn with Thevinin's theo



⇒ Thevinin's resistance at D_1 & D_2 $R_1 = Rth = \frac{R_2 R_C}{R_2 + R_C}$ of $V_S = V_C = 0$

⇒ Thevenin's voltage is calculated using V_S & V_C first we using

⇒ V_S & $V_C = 0$ Thevinin's equivalent voltage using V_S of point A

$$V_{AS} = \frac{R_C}{R_C + R_2} V_S \quad \left(\because \alpha = \frac{R_C}{R_C + R_2} \right)$$

$$= \alpha V_S$$

⇒ $V_S = 0$, & $V_C \neq 0$ $V_{AC} = \frac{R_2}{R_C + R_2} V_C \left(\because \frac{R_C}{R_C + R_2} = \alpha \right)$

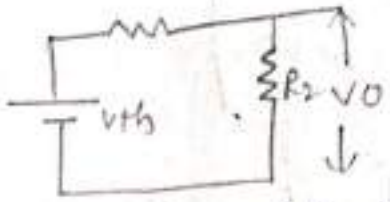
$$= (1 - \alpha) V_C \left[1 - \alpha = 1 - \frac{R_C}{R_C + R_2} = \frac{R_C + R_2 + R_C}{R_C + R_2} = \frac{R_2}{R_C + R_2} \right]$$

⇒ each diode has been replaced by its piece wise linear mod-el i.e, a battery of V_γ Equal to the affect voltage in series with a resistance R_S equal to the diode forward resistance.

⇒ By using R_1 & R_f equivalent resistance as $R_S = R_1 + R_f$.

⇒ To the calculation of gain apply thevenin's equivalent circuit at R_2 the circuit as

⇒ V_C voltage are forward biased D_1 & D_2 and V_S is directly passed to V_O & at the transmission period apply thevenin's Equivalent circuit with respect to V_C V_S.



Vc are Assuming of '0'. RS & R_3 are in parallel for the calculation of thevinin's resistance.

$$R_{th} = \frac{R_3 R_1}{R_1 + R_3} = \frac{R_3}{2}$$

$$\alpha V_S = \frac{R_3}{R_2 + R_3/2} = \left(\frac{R_C}{R_C + R_1}\right) \cdot \frac{R_2}{(R_2 + R_3/2)} \cdot V_S$$

$$A = \frac{V_0}{V_S} = \left(\frac{R_C}{R_C + R_1}\right) \cdot \frac{R_2}{R_2 + R_3/2}$$ → Gain of bidirectional sampling Gate.

Control voltages $V_c$min & $V_n$min :-

⇒ D_1 & D_2 are forward biased & $V_S = 0V$ i.e $V_0 = 0V$.

⇒ Let V_S is applied with positive going signal current of D_1 is high compared to current of D_2 as V_S increases in positive direction D_1 current increases in forward bias of conditions & D_2 current decreases and getting into reverse bias conditions & hence diff-ent current flows through D_2

⇒ V_0 w.r.to D_1 K.B = V_0 w.r.to D_2 K.B

$$\frac{R_L}{R_L + R_3}(\alpha V_S + (1-\alpha) V_S) = \alpha V_S (1-\alpha) V_S$$

$$\frac{R_L}{R_L + R_3}[1-\alpha] V_c + (1-\alpha) V_c = \alpha V_S - \alpha V_S \frac{R_2}{R_L + R_3}$$

$$(1-\alpha) V_S \left[1 + \frac{R_2}{R_L + R_3}\right] = \alpha V_S \left[1 - \frac{R_L}{R_2 + R_3}\right]$$

$$(1-\alpha) V_c \left[\frac{R_3 + 2R_2}{R_L + R_3}\right] = \alpha V_S \left[\frac{R_3}{R_L + R_3}\right]$$

$$(1-\alpha) V_c (R_3 + 2R_L) = \alpha V_S \cdot R_3$$

$$\frac{R_2}{R_2} V_c (R_3 + 2R_2) = \frac{R_C}{R_C + R_2} \cdot R_3 V_S$$

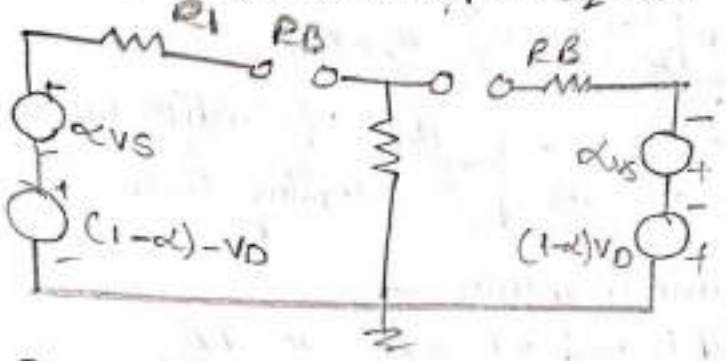
$$V_{C(min)} = \left(\frac{R_C}{R_2}\right)\left(\frac{R_3}{R_3+2R_2}\right)V_S$$

⇒ A minimum control voltage ($V_{c(min)}$) is required to keep both the diodes OFF when no sampling takes place

⇒ Apply KVL across diode D_2

$$V_P = -\alpha V_S + (1-\alpha)V_D$$

Worst case condition V_{D_1} & $V_{D_2} = 0V$



$$0 = -\alpha V_S + (1-\alpha)V_n$$

$$\alpha V_S = (1-\alpha)V_n$$

$$\Rightarrow (1-\alpha)V_n = \alpha V_S$$

$$\frac{R_2}{R_C+R_2} V_n = \frac{R_C}{R_C+R_2}$$

$$V_n = \frac{R_C}{R_2} V_S$$

$$V_{n\,min} = \frac{R_C}{R_2} \cdot V_S$$

In practice for safety reasons larger values of $V_{C\,min}$ of $V_{o\,min}$ are choosen compared to the above minimum values.

⇒ A larger value of $V_{C(min)}$ improves the linearity in addition to safety.

Disadvantages of 2 diode bidirectional sampling gate:-

1) It's gain is low.
2) It is sensitive to control voltage imbalance
3) There is a possibility that V_n min may be excessive in V_n min > V_c min.
4) there may be appreciable leakage through the diode capacitance.
5) To overcome these drawbacks we are using 4 diode sampling gates.

Course materials like Notes, PPT's, etc.

1. **https://drive.google.com/file/d/1v7lNhVV6N0-8jW8tj-XWGNVaJq1f5kPx/view?usp=classroom_web&authuser=0**
2. **https://drive.google.com/file/d/1O-rBF5vkwmqDJ74MCgIJ5sfgo1XqjPpv/view?usp=classroom_web&authuser=0**
3. **https://drive.google.com/file/d/12uidusPWRLwz9kxBYq2xtxPNv2A52J6j/view?usp=classroom_web&authuser=0**
4. **https://drive.google.com/file/d/1ACFFlnp3PJU4_tszP8XN4KPODViyGf7v/view?usp=classroom_web&authuser=0**
5. **https://drive.google.com/file/d/1t7ssEFZKKEfS9zGfAk4yPhtT8rw89fuV/view?usp=classroom_web&authuser=0**