Department of Electronics and Communication Engineering

Course File

LINEAR AND DIGITAL IC APPLICATIONS

(Course Code: EC404PC)

II B.Tech II Semester

2023-24

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Anurag ENGINEERING COLLEGE (An Autonomous Institution)

Department of Electronics and Communication Engineering

LINEAR AND DIGITAL IC APPLICATIONS

Check List

Department of Electronics and Communication Engineering

Int. Marks:40 Ext. Marks:60 Total Marks:100

LINEAR AND DIGITAL IC APPLICATIONS

Course Code:EC404PC **L/T/P/C:3/0/0/3**
II Year II Semester

UNIT - I

Operational Amplifier: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Modes of Operation-Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT - II

Op-Amp, IC-555 & IC565 Applications: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators – Triangular, Sawtooth, Square Wave, IC555 Timer-Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL-Block Schematic, principle and Applications.

UNIT - III

Data Converters: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs – Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT - IV

Combinational Logic ICs: Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor, Magnitude Comparators.

UNIT - V

Sequential Logic IC’s and Memories: Familiarity with commonly available 74XX & CMOS40XX Series ICs - All Types of Flip-flops, Synchronous Counters, Decade Counters, Shift Registers.

Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXT BOOKS:

1. Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
2. Floydand Jain- Digital Fundamentals, 8th Ed., PearsonEducation,2005.

REFERENCE BOOKS:

1. D. Roy Chowdhury – Linear Integrated Circuits, New Age International(p)Ltd, 2nd Ed., 2003.
2. John. F. Wakerly – Digital Design Principles and Practices, 3rdEd., Pearson, ,2009.
3. Salivahana -Linear Integrated Circuits and Applications, TMH, 2008.
4. William D.Stanley- Operational Amplifiers with Linear Integrated Circuits, 4thEd., Pearson Education India, 2009.

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Timetable

II B.Tech. II Semester – LDIC (A&B Sections)

Day/Hour	09:30AM - 10:20AM	10:20AM- 11:10AM	11:20AM – 12:10 PM	12:10 PM - 01:00 PM	01:40 PM -02:25PM	02:25 PM-03:10 PM	03:15 PM-04:00 PM
Monday		LDIC-B				LDIC-B	LDIC -A
Tuesday		LDIC-A	LDIC-B				
Wednesday					LDIC-A		
Thursday	LDIC-B		LDIC-A				
Friday	LDIC-A			LDIC-B			
Saturday					LDIC-A		

Department of Electronics and Communication Engineering

Vision of the Institute

To be a premier Institute in the country and region for the study of Engineering, Technology and Management by maintaining high academic standards which promotes the analytical thinking and independent judgment among the prime stakeholders, enabling them to function responsibly in the globalized society.

Mission of the Institute

To be a world-class Institute, achieving excellence in teaching, research and consultancy in cutting-edge Technologies and be in the service of society in promoting continued education in Engineering, Technology and Management.

Quality Policy

To ensure high standards in imparting professional education by providing world-class infrastructure, top-quality-faculty and decent work culture to sculpt the students into Socially Responsible Professionals through creative team-work, innovation and research

Vision of the Department

Our vision is to develop the department into a full-fledged centre of learning in various fields of Electronics & Communication Engineering keeping in view the latest development.

Mission of the Department

The Mission of the department is to turn out full-fledged Engineers in the field of Electronics & Communication Engineering with an overall back-ground suitable for making a successful career either in industry/research or higher education in India and abroad. To inculcate professional behavior, strong ethical values, innovative research capabilities and leadership abilities in the young minds so as to work with a commitment to the progress of the nation.

Department of Electronics and Communication Engineering

Program Educational Objectives (B.Tech. – ECE)

Graduates will be able to

PEO 1	**:**	Excel in professional career & higher education, by acquiring knowledge in related fields of Electronics & Communication Engineering.
PEO 2	**:**	Exhibit leadership in their profession, through technological ability and contemporary knowledge for solving real life problems appropriately that are technically sound, economically feasible & socially acceptable.
PEO 3	**:**	Adapt to the emerging technologies for sustenance by exhibiting professionalism, ethical attitude & communication skills in their relevant areas of interest by engaging in lifelong learning.

Department of Electronics and Communication Engineering

Program Outcomes (B.Tech. – ECE)

At the end of the Program, a graduate will have the ability to

PO 1	:	An ability to apply knowledge of mathematics, science, fundamentals of engineering to solve electronics and communication engineering problems.
PO 2	:	An ability to identify, formulate and analyze and solve complex electronics and communication Engineering using the first principles of mathematics and engineering sciences.
PO 3	:	An ability to develop solutions to electronics and communication systems to meet the specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.
PO 4	:	An ability to design and perform experiments of electronic circuits and systems, analyze and interpret data to provide valid conclusions.
PO 5	:	An ability to learn, select and apply appropriate techniques, resources and modern engineering tools including prediction and modelling, to complex electronics and communication systems.
PO 6	:	An ability to assess the knowledge of contemporary issues to the societal responsibilities relevant to the professional practice.
PO 7	:	An ability to understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate knowledge for the need of sustainable development.
PO 8	:	An ability to demonstrate the understanding of professional, ethical responsibilities and norms of engineering practice.
PO 9	:	An ability to function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.
PO 10	:	An ability to communicate effectively with the engineering community and with society at large.
PO 11	:	An ability to demonstrate knowledge and understanding of engineering and management principles and apply these to manage projects.
PO 12	:	An ability to recognize the need for, and engage in lifelong learning in the broadest context of technological change.

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COURSE OBJECTIVES

On completion of this Subject/Course the student shall be able to:

S.No	Objectives
1	To introduce the basic building blocks of linear integrated circuits.
2	To introduce the theory and applications of Analog multipliers and PLL.
3	To introduce the concept sine waveform generation and introduce some special Function ICs.
4	To understand and implement the working of basic digital circuits.

COURSE OUTCOMES

The expected outcomes of the Course/Subject are:

S.No	Outcomes
1.	A thorough understanding of operational amplifiers with linear integrated circuits.
2.	Attain the knowledge of functional diagrams and design applications of IC555 and IC565.
3.	Acquire the knowledge and design the Data converters.
4.	Choose the proper digital integrated circuits by knowing their characteristics.
5.	Acquire the knowledge of sequential logic ICs and memories

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Note: Please refer to Bloom's Taxonomy, to know the illustrative verbs that can be used to state the outcomes.

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GUIDELINES TO STUDY THE COURSE / SUBJECT

Course Design and Delivery System (CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

- Understand the principles of Learning
- Understand the psychology of students
- Develop instructional objectives for a given topic
- Prepare course, unit and lesson plans
- Understand different methods of teaching and learning
- Use appropriate teaching and learning aids
- Plan and deliver lectures effectively
- Provide feedback to students using various methods of Assessments and tools of Evaluation
- Act as a guide, advisor, counselor, facilitator, motivator and not just as a teacher alone

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COURSE SCHEDULE

The Schedule for the whole Course / Subject is:

S. No.	Description	Duration (Date)		Total No. of Periods
		From	To	
1.	**UNIT - I** Operational Amplifier: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Modes of Operation-Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.	05.02.2024	23.02.2024	12
2.	**UNIT - II** Op-Amp, IC-555 & IC565 Applications: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators – Triangular, Sawtooth, Square Wave, IC555 Timer-Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL-Block Schematic, principle and Applications.	26.02.2024	19.03.2024	13
3.	**UNIT - III** Data Converters: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs – Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.	21.03.2024	25.04.2024	13
4.	**UNIT - IV** Combinational Logic ICs: Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor, Magnitude Comparators.	26.04.2024	10.05.2024	12
5.	**UNIT - V** Sequential Logic IC's and Memories: Familiarity with commonly available 74XX & CMOS40XX Series ICs - All Types of Flip-flops, Synchronous Counters, Decade Counters, Shift Registers. Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.	03.06.2024	11.06.2024	11

Total No. of Instructional periods available for the course: 62 Hours

Department of Electronics and Communication Engineering

SCHEDULE OF INSTRUCTIONS - COURSE PLAN

Unit No.	Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1.	1	05.02.2024	1	UNIT - I: Ideal and Practical Op-Amp, Op-Amp Characteristics	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	2	06.02.2024	1	DC and AC Characteristics, Features of 741 Op-Amp	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	3	07.02.2024 & 08.02.2024	2	Modes of Operation-Inverting	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	4	09.02.2024 & 12.02.2024	2	Non-Inverting, Differential	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	5	13.02.2024 & 14.02.2024	2	Instrumentation Amplifier, AC Amplifier	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	6	16.02.2024	1	Differentiators, Integrators, Comparators	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	7	19.02.2024	1	Schmitt Trigger	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	8	20.02.2024 & 21.02.2024	2	Voltage Regulators- Three Terminal Voltage Regulators	1 1	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
2.	1	22.02.2024	1	UNIT - II : Op-Amp, IC-555 & IC565 Applications	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	2	23.02.2024	1	Introduction to Active Filters, Characteristics of Band pass, Band reject, All Pass Filters	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.

	3	23.02.2024 & 24.02.2024	2	Analysis of 1st order LPF, HPF Butterworth Filters	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	4	26.02.2024	1	Triangular, Sawtooth, Square Wave, Generators	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	5	27.02.2024 & 01.03.2024	2	IC555 Timer-Functional Diagram	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	6	02.03.2024	1	Monostable operation	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	7	04.03.2024 & 05.03.2024	2	Astable Operation	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	8	05.03.2024	1	IC565 PLL-Block Schematic diagram	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	9	07.03.2024 & 11.03.2024	2	PLL principle and Applications	2 2	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
3.	1	14.03.2024	1	**UNIT - III** Data Converters	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	2	15.03.2024	1	Different types of DACs,	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	3	16.03.2024 & 18.03.2024	2	Weighted resistor DAC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	4	19.03.2024 & 21.03.2024	2	R-2R ladder DAC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	5	23.03.2024	1	Inverted R-2R DAC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	6	23.03.2024 & 26.03.2024	2	Different Types of ADCs, Parallel Comparator Type ADC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.

	7	28.03.2024	1	Counter Type ADC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	8	30.03.2024 & 08.04.2024	2	Dual Slope ADC	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	9	10.04.2024	1	DAC and ADC Specifications	3 3	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
4	1	10.04.2024	1	**UNIT – IV**: Combinational Logic Ics	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	2	15.04.2024	1	Specifications and of TTL-74XX & CMOS 40XX, Applications of TTL-74XX & CMOS 40XX	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	3	16.04.2024	1	Code Converters: Decoders	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	4	18.04.2024	1	LED Decoders with Drivers	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	5	19.04.2024 & 20.04.2024	2	Encoders	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	6	22.04.2024	1	Priority Encoders	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	7	23.04.2024	1	Multiplexers	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	8	24.04.2024 & 25.04.2024	2	Priority Generators/Checkers	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	9	26.04.2024	1	Parallel Binary Adder/Subtractor	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	10	27.04.2024	1	Magnitude Comparators	4 4	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
5	1	29.04.2024	1	**UNIT – V**: Sequential Logic IC's and Memories	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.

	2	30.04.2024	1	Familiarity with commonly available 74XX Series Ics	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	3	01.05.2024	1	All Types of Flip-flops, S-R Flip-flop	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	4	02.05.2024	1	J-K Flip-flop	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	5	06.05.2024	2	Synchronous Counters	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	6	04.06.2024	1	Decade Counters	5 5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	7	05.06.2024	1	Shift Registers	5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	8	07.06.2024	1	Memories- ROM Architecture	5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.
	9	10.06.2024 & 11.06.2024	2	Memories- RAM Architecture	5	Ramakanth A. Gayakwad - Op-Amps & Linear ICs, PHI, 2003.

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Date:

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Date:

Note:

1. Ensure that all topics specified in the course are mentioned.
2. Additional topics covered, if any, may also be specified in bold.
3. Mention the corresponding course objective and outcome numbers against each topic.

Department of Electronics and Communication Engineering

LESSON PLAN (U-I)

Lesson No: 03, 04 Duration of Lesson: 1hr 40 min

Lesson Title: Op-Amp, Modes of Operation-Inverting, Non-Inverting, Differential amplifiers

Instructional / Lesson Objectives:

- To make students understand OP-AMP and modes of operation
- To familiarize students on inverting and non-inverting, differential
- To understand students the concept of IC 741 OP AMP and its features

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 80 min for the lecture delivery 15 min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. What are the different modes of operation of operational amplifier and explain with neat diagrams.

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LESSON PLAN (U-II)

Lesson No: 02, 03 Duration of Lesson: 1hr 40min

Lesson Title: Analysis of 1st order LPF, HPF Butterworth Filters

Instructional / Lesson Objectives:

- To make students understand filter characteristics and their concept
- To familiarize students on 1st order LPF, HPF Butterworth Filters
- To understand students the concept of Butterworth Filters

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10 min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

1. Design first order high pass filter at a higher cut off frequency of 1khz with a pass band gain of 2

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LESSON PLAN (U-III)

Lesson No: 06, 07 Duration of Lesson: 1hr 40min

Lesson Title:

Instructional / Lesson Objectives:

- To make students understand the concept of analog to digital converters.
- To familiarize students on Different Types of ADCs,
- To understand students Different Types of ADCs, Parallel Comparator Type ADC, Counter Type ADC, Dual Slope ADC

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

Refer assignment-III & tutorial-III sheets.

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LESSON PLAN (U-IV)

Lesson No: 06, 07 Duration of Lesson: 1hr 40min

Lesson Title: Code Converters, Decoders, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Priority Generators/Checkers

Instructional / Lesson Objectives:

- To make students understand the concept of. Code Converters
- To familiarize students on Decoders, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Priority Generators/Checkers

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

Refer assignment-IV & tutorial-IV sheets.

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LESSON PLAN (U-V)

Lesson No: 03, 04 Duration of Lesson: 1hr 40min

Lesson Title: All Types of Flip-flops, Memories, Synchronous Counters

Instructional / Lesson Objectives:

- To make students understand the concept of counters
- To familiarize students on synchronous counters

Teaching AIDS : PPTs, Digital Board
Time Management of Class :

5 mins for taking attendance 10 for revision of previous class 75 min for lecture delivery 10min for doubts session

Assignment / Questions:
(Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..)

Refer assignment-V& tutorial-V sheets.

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ASSIGNMENT – 1

This Assignment corresponds to Unit No. 1

Question No.	Question	Objective No.	Outcome No.
1	Describe the working of Practical differentiator circuit and derive the expression for output voltage.	1	1
2	What are the different modes of operation of operational amplifier and explain with neat diagrams.	1	1

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ASSIGNMENT – 2

This Assignment corresponds to Unit No. 2

Question No.	Question	Objective No.	Outcome No.
1	Draw and explain the functional diagram of 555 timer.	2	2
2	Design first order high pass filter at a higher cut off frequency of 1khz with a pass band gain of 2	2	2

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Department of Electronics and Communication Engineering

ASSIGNMENT – 3

This Assignment corresponds to Unit No. 3

Question No.	Question	Objective No.	Outcome No.
1	Draw and explain the circuit opration of an inverted R-2R DAC.	3	3
2	Find out step size and analog output for 4 bit binary weighted resister DAC when inut is 0111 and 1111, assume Vref = +5v.	3	3

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ASSIGNMENT – 4

This Assignment corresponds to Unit No. 4

Question No.	Question	Objective No.	Outcome No.
1	Explain 3 to 8 decoder with IC and logic diagram.	4	4
2	Explain about encoders and priority encoder.	4	4

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ASSIGNMENT – 5

This Assignment corresponds to Unit No. 5

Question No.	Question	Objective No.	Outcome No.
1	Explain with the help of neat diagram the simple structure of ROM.	4	4
2	Draw and explain the 4 bit Johnson counter.	4	4

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Department of Electronics and Communication Engineering

TUTORIAL – 1

This tutorial corresponds to Unit No. 1 (Objective Nos.: 1, Outcome Nos.: 1)

Q1. Find the output voltage of an ideal op-amp. If V1 and V2 are the two input voltages.

a) VO= V1-V2 b) VO= A×(V1-V2) c) VO= A×(V1+V2) d) VO= V1×V2

Q2. What is the use of notch and dot in DIP ICs?

a) Determine the pin configuration
b) Designed to represent device type
c) Represent property of IC
d) Find the pin numb

Q3. Which of the following electrical characteristics is not exhibited by an ideal op-amp?

a) Infinite voltage gain
b) Infinite bandwidth
c) Infinite output resistance
d) Infinite slew rate

Q4. Define op-amp?

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TUTORIAL – 2

This tutorial corresponds to Unit No. 2 (Objective Nos.: 2, Outcome Nos.: 2)

Q1. The gain of the first order low pass filter

a) Increases at the rate 20dB/decade
b) Increases at the rate 40dB/decade
c) Decreases at the rate 20dB/decade
d) Decreases at the rate 40dB/decade

Q2. Determine the time period of a monostable 555 multivibrator

a) T = 0.33RC
b) T = 1.1RC
c) T = 3RC
d) T = RC

Q3. How does a monostable multivibrator used as frequency divider?

a) Using square wave generator
b) Using triangular wave generator
c) Using saw tooth wave generator
d) Using sine wave generator

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TUTORIAL SHEET – 3

This tutorial corresponds to Unit No. 3 (Objective Nos.: 3, Outcome Nos.: 3)

Q1. Why the switches used in weighted resistor DAC are of single pole double throw (SPDT) type?

a) To connect the resistance to reference voltage
b) To connect the resistance to ground
c) To connect the resistance to either reference voltage or ground
d) To connect the resistance to output

Q2 What is the disadvantage of binary weighted type DAC?

a) Require wide range of resistors
b) High operating frequency
c) High power consumption
d) Slow switching

Q3. Find out the integrating type analog to digital converter?

a) Flash type converter
b) Tracking converter
c) Counter type converter
d) Dual slope ADC

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TUTORIAL – 4

This tutorial corresponds to Unit No. 4 (Objective Nos.: 3, Outcome Nos.: 3)

Q1. Code is a symbolic representation of _____

a) Discrete information
b) Continuous information
c) Decimal information into binary
d) Binary information into decimal

Q2. If we record any music in any recorder, such types of process is called _____

a) Multiplexing
b) Encoding
c) Decoding
d) Demultiplexing

Q3. How many select lines would be required for an 8-line-to-1-line multiplexer?

a) 2
b) 4
c) 8
d) 3

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TUTORIAL SHEET – 5

This tutorial corresponds to Unit No. 5 (Objective Nos.: 5, Outcome Nos.: 5)

Q1. Which of the following options represent the synchronous control inputs in an S – R flip flop?

a) S b) R c) BOTH S&R d) CLOCK

Q2.What gate is placed between clock input and the input of AND gate to convert a positive level triggered flip – flop to a negative level triggered flip – flop?

a) NOR gate b) NAND gate c) NOT gate d) BUFFER

Q3. A counter circuit is usually constructed of

a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form

Signature of HOD

Date:

Signature of faculty

Date:

Department of Electronics and Communication Engineering

EVALUATION STRATEGY

Target (s)

a. Percentage of Pass : 95%

Assessment Method (s) (Maximum Marks for evaluation are defined in the Academic Regulations)

a. Daily Attendance
b. Assignments
c. Online Quiz (or) Seminars
d. Continuous Internal Assessment
e. Semester / End Examination

List out any new topic(s) or any innovation you would like to introduce in teaching the subjects in this semester

Case Study of any one existing application

Signature of HOD

Date:

Signature of faculty

Date:

Department of Electronics and Communication Engineering

COURSE COMPLETION STATUS

Actual Date of Completion & Remarks if any

Units	Remarks	Objective No. Achieved	Outcome No. Achieved
Unit 1	completed on 23.02.2024	1	1
Unit 2	completed on 19.03.2024	2	2
Unit 3	completed on 25.04.2024	3	3
Unit 4	completed on 10.05.2024	4	4
Unit 5	completed on 11.06.2024	5	5

Signature of HOD

Date:

Signature of faculty

Date:

Department of Electronics and Communication Engineering

Mappings

1. Course Objectives-Course Outcomes Relationship Matrix

(Indicate the relationships by mark "X")

Course-Outcomes / Course-Objectives	1	2	3	4	5
1	H	M			
2		H			
3			H		
4				H	M
5				M	H

2. Course Outcomes-Program Outcomes (POs) & PSOs Relationship Matrix

(Indicate the relationships by mark "X")

P-Outcomes / C-Outcomes	a	b	c	d	e	f	g	h	i	j	k	l	PSO 1	PSO 2	PSO 3
1	H	H	M	L									H	M	L
2	H	H	H	L										H	M
3	H	H	H	L										H	M
4	H	H	M	L											L
5	H	H	H	M											L

Department of Electronics and Communication Engineering

Rubric for Evaluation

Performance Criteria	Unsatisfactory	Developing	Satisfactory	Exemplary
	1	2	3	4
Research & Gather Information	Does not collect any information that relates to the topic	Collects very little information some relates to the topic	Collects some basic Information most relates to the topic	Collects a great deal of Information all relates to the topic
Fulfill team role's duty	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.
Share Equally	Always relies on others to do the work.	Rarely does the assigned work - often needs reminding.	Usually does the assigned work - rarely needs reminding.	Always does the assigned work without having to be reminded
Listen to other team mates	Is always talking—never allows anyone else to speak.	Usually doing most of the talking-- rarely allows others to speak	Listens, but sometimes talks too much.	Listens and speaks a fair amount.

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II B.TECH IV SEMESTER I MID EXAMINATIONS - APRIL 2024

Branch : B.Tech. (ECE) **Max. Marks: 30**
Date : 02 - Apr - 2024 AN **Time: 120 Minutes**
Subject : Linear and Digital IC Applications,EC404PC

PART - A

ANSWER ALL QUESTIONS **10 X 1 M = 10 M**

Q.No	Question		CO	BTL
1.	What is the slew rate of ideal op-amp? (A). zero (B). infinity (C). 1 (D). None of the mentioned	( )	CO1	1
2.	What happens due to mismatch between two input terminals in an op-amp? (A). Input offset voltage (B). Output offset voltage (C). Bothe the input and output offset voltage (D). None of the mentioned	( )	CO1	1
3.	Which of the following electrical characteristics is not exhibited by an ideal op-amp? (A). Infinite voltage gain (B). Infinite bandwidth (C). Infinite output resistance (D). Infinite slew rate	( )	CO1	1
4.	What is the best choice of IC package used for experimental purpose? (A). Flat pack (B). Transistor pack (C). DIP package (D). Metal can package	( )	CO1	1
5.	Draw the ciruit diagram of Sawtooth wave generator	( )	CO2	1
6.	Define filter	( )	CO2	2
7.	Determine the time period of a monostable 555 multivibrator (A). T = 0.33RC (B). T = 1.1RC (C). T = 3RC (D). T = RC	( )	CO2	1
8.	what are the applications of IC 555 timer	( )	CO2	1
9.	A binary input 000 is fed to a 3bit DAC/ADC. The resultant output is 101. Find the type of error? (A). Settling error (B). Gain error (C). Offset error (D). Linearity error	( )	CO3	1
10.	How to overcome the limitation of binary weighted resistor type DAC? (A). Using R-2R ladder type DAC (B). Multiplying DACs (C). Using monolithic DAC (D). Using hybrid DAC	( )	CO3	1

PART - B

ANSWER ANY FOUR **4 X 5 M = 20 M**

Q.No	Question	CO	BTL
11.	Write about AC and DC characteristics, features of IC 741 Op-Amp.	CO1	3
12.	With neat sketch explain the operation of comparator and Schmitt trigger using Op- Amp.	CO1	2
13.	Explain the operation of Astable multivibrator using 555 timer.	CO2	3
14.	Draw the block diagram of PLL and explain the importance of each block.	CO2	3

15.	Find out step size and analog output for 4 bit binary weighted resister DAC when input is 0111 and 1111, assume Vref = +5v.	CO3	4
16.	Draw and explain the circuit opration of an inverted R-2R DAC.	CO3	3

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II B.TECH IV SEMESTER II MID EXAMINATIONS - JUNE 2024

Branch : B.Tech. (ECE) **Max. Marks : 30M**
Date : 19-Jun-2024 Session : Afternoon **Time : 120 Min**
Subject : Linear and Digital IC Applications,EC404PC

PART - A

ANSWER ALL THE QUESTIONS **10 X 1M = 10M**

Q.No	Question	CO	BTL
1.	What is the principle of ADC?	CO3	2
2.	Which of the following method is employed for ADC? ( ) (A). Ladder network (B). Successive approximation type (C). PWM type (D). None of the mentioned	CO3	1
3.	What is code converter?	CO4	1
4.	A code converter is a logic circuit that _____ ( ) (A). Inverts the given input (B). Converts into decimal number (C). Converts data of one type into another type (D). Converts to octal	CO4	2
5.	List out the applications of multiplexer	CO4	2
6.	What is Demultiplexer?	CO4	1
7.	Give the comparison between synchronous & Asynchronous sequential circuits?	CO5	1
8.	Master slave flip flop is also referred to as? ( ) (A). Level triggered flip flop (B). Pulse triggered flip flop (C). Edge triggered flip flop (D). Edge-Level triggered flip flop	CO5	1
9.	The full form of SIPO is _____ ( ) (A). Serial-in Parallel-out (B). Parallel-in Serial-out (C). Serial-in Serial-out (D). Serial-In Peripheral-Out	CO5	2
10.	A flip flop stores _____ ( ) (A). 10 bit of information (B). 1 bit of information (C). 2 bit of information (D). 3-bit information	CO5	1

PART - B

ANSWER ANY FOUR **4 X 5M = 20M**

Q.No	Question	CO	BTL
11.	Explain the operation of Dual slope ADC with diagram	CO3	3
12.	Write about parallel comparator type ADC	CO3	3
13.	what is the parity generator and checker and explain with diagrams	CO4	3
14.	Explain about the four bit magnitude comparator ?	CO4	3
15.	Draw the circuit diagram of a 4 bit ripple counter. Explain its working.	CO5	3
16.	Explain the archItecture of RAM	CO5	3

Department of Electronics and Communication Engineering

S.No.	H.T.No.	Name of the Student	Mid - I Marks (30)	Mid - II Marks (30)	Avg of Mid-I & Mid-II (A)	Assignment - I (5)	Assignment - II (5)	Avg of Assg.-I & Assg.-II (B)	Viva Voce (5) (C)	Total (A+B+C)
1	22C11A0401	VANKA ADARSH REDDY	16	14	15	5	5	5	5	25
2	22C11A0402	PILLALAMARRI AJAY	17	20	19	5	5	5	5	29
3	22C11A0404	THUNKOJU AKHIL	28	29	29	5	5	5	5	39
4	22C11A0405	GADDAM AKHILA	23	15	19	5	5	5	5	29
5	22C11A0407	AITHAGANI ANUSHA	28	29	29	5	5	5	5	39
6	22C11A0408	KARISHA ASHOK	18	12	15	5	5	5	5	25
7	22C11A0409	KILARU BHASWANTH KUMAR	18	19	19	5	5	5	5	29
8	22C11A0410	ERLA BHAVANA	26	29	28	5	5	5	5	38
9	22C11A0411	BANOTHU CHANDRA SHEKAR	23	12	18	5	5	5	5	28
10	22C11A0413	GUGULOTHU DIVYA	27	27	27	5	5	5	5	37
11	22C11A0414	KOTHAPALLI DIVYA JYOTHI	21	21	21	5	5	5	5	31
12	22C11A0415	THALLA GAYATHRI	28	28	28	5	5	5	5	38
13	22C11A0416	GODHUMALA GOPICHAND	26	28	27	5	5	5	5	37
14	22C11A0417	BHUKYA HARSHITHA	26	26	26	5	5	5	5	36
15	22C11A0418	REDDYMALLA JANAKI RAM REDDY	22	11	17	5	5	5	5	27
16	22C11A0419	SHAIK JASMINE	26	21	24	5	5	5	5	34

17	22C11A0420	JANAPATI JYOSHNA	26	26	26	5	5	5	5	36
18	22C11A0421	DHARAVATH KARTHIK	22	24	23	5	5	5	5	33
19	22C11A0422	JONNALAGADDA KAVYA	22	26	24	5	5	5	5	34
20	22C11A0423	JONNALAGADDA KAVYA SREE	23	26	25	5	5	5	5	35
21	22C11A0424	SHAIK KHATIJA	30	30	30	5	5	5	5	40
22	22C11A0425	KONDRU LAKSHMI	AB	19	10	5	5	5	5	20
23	22C11A0426	BODA LIKHITHA	28	28	28	5	5	5	5	38
24	22C11A0427	KUNDURU LIKHITHA REDDY	28	29	29	5	5	5	5	39
25	22C11A0428	CHINTHAKUNTLA LOKESH REDDY	26	26	26	5	5	5	5	36
26	22C11A0429	KOLLURI MADHU	14	16	15	5	5	5	5	25
27	22C11A0430	GUJJULA MAMATHA	AB	AB	0	0	0	0	0	0
28	22C11A0431	MADASU MAMATHA	AB	AB	0	0	0	0	0	0
29	22C11A0432	CHINNAM MANASA	13	13	13	5	5	5	5	23
30	22C11A0433	NANNEBOINA MEGHANA	28	29	29	5	5	5	5	39
31	22C11A0434	BHUKYA MOKSHAGNA	28	24	26	5	5	5	5	36
32	22C11A0435	GUNDLA NANDINI	29	30	30	5	5	5	5	40
33	22C11A0436	AKULA NARESH	24	30	27	5	5	5	5	37
34	22C11A0437	KODI NAVEEN	15	16	16	5	5	5	5	26
35	22C11A0438	POLOJU NAVEEN	22	23	23	5	5	5	5	33
36	22C11A0439	VARRA NAVEEN REDDY	20	20	20	5	5	5	5	30

37	22C11A0440	MALLELA NAVYA	26	29	28	5	5	5	5	38
38	22C11A0441	PAGADALA NAVYA	30	30	30	5	5	5	5	40
39	22C11A0442	MADDURI NICHITHA	30	24	27	5	5	5	5	37
40	22C11A0443	KOVVURI NIKHIL	12	13	13	5	5	5	5	23
41	22C11A0444	GUDIPATI NIKHIL SAI KUMAR	20	17	19	5	5	5	5	29
42	22C11A0445	NAGIREDDY NIRANJAN REDDY	29	28	29	5	5	5	5	39
43	22C11A0446	ENUGURTHI NITHIN	18	12	15	5	5	5	5	25
44	22C11A0447	BANALA NITHIN VAMSHI	28	23	26	5	5	5	5	36
45	22C11A0448	UDARI NITHISH KUMAR	18	16	17	5	5	5	5	27
46	22C11A0449	AKARAPU POOJITHA	27	29	28	5	5	5	5	38
47	22C11A0450	BOLLAKA POOJITHA	28	29	29	5	5	5	5	39
48	22C11A0451	YARAGANI PRAJVAL	22	25	24	5	5	5	5	34
49	22C11A0453	MAMIDI PRIYANKA	27	29	28	5	5	5	5	38
50	22C11A0454	THOKALA PURUSHOTHAM	14	15	15	5	5	5	5	25
51	22C11A0455	MOHAMMAD RAFI	22	21	22	5	5	5	5	32
52	22C11A0456	NUKALA RAJAGOPAL REDDY	28	29	29	5	5	5	5	39
53	22C11A0457	K RAJU	28	30	29	5	5	5	5	39
54	22C11A0458	PANGOTH RAM KUMAR	26	24	25	5	5	5	5	35
55	22C11A0459	SHEELAM RAMAKANTH	20	17	19	5	5	5	5	29
56	22C11A0460	BANOTHU RAVI	25	28	27	5	5	5	5	37

Department of Electronics and Communication Engineering

S.No.	H.T.No.	Name of the Student	Mid - I Marks (30)	Mid - II Marks (30)	Avg of Mid-I & Mid-II (A)	Assignment - I (5)	Assignment - II (5)	Avg of Assg.-I & Assg.-II (B)	Viva Voce (5) (C)	Total (A+B+C)
1	22C11A0461	KOTIKA RAVI KIRAN	25	29	27	5	5	5	5	37
2	22C11A0462	SHAIK RESHMA	22	21	22	5	5	5	5	32
3	22C11A0463	BADETI SAI	15	19	17	5	5	5	5	27
4	22C11A0464	SAMPATHARAO SAI KUMAR	17	27	22	5	5	5	5	32
5	22C11A0465	KALLA SAI MANOJKUMAR	22	29	26	5	5	5	5	36
6	22C11A0466	KANDULA SAIKIRAN	12	18	15	5	5	5	5	25
7	22C11A0467	SHAIK SAMEER	21	24	23	5	5	5	5	33
8	22C11A0469	ANANTHARAPU SANJAN	18	19	19	5	5	5	5	29
9	22C11A0470	PALLY SANTHOSH REDDY	12	18	15	5	5	5	5	25
10	22C11A0471	SHAIK SHAFIQ	20	26	23	5	5	5	5	33
11	22C11A0472	N SHARATH CHANDRA	30	30	30	5	5	5	5	40
12	22C11A0473	BATTULA SHARATH GOPAL	15	12	14	5	5	5	5	24
13	22C11A0474	KUMBHAM SHIRISHA	19	27	23	5	5	5	5	33
14	22C11A0475	PANUGOTH SHIVA	19	21	20	5	5	5	5	30
15	22C11A0476	BOLISETTY SHIVA SHANKAR	11	16	14	5	5	5	5	24
16	22C11A0477	CHENNAKESHAVA SHREYA	23	24	24	5	5	5	5	34
17	22C11A0478	BHUKYA SIDDU NAIK	19	19	19	5	5	5	5	29
18	22C11A0479	MEKALA SINDHU	29	29	29	5	5	5	5	39
19	22C11A0480	LAVORI SRAVANI	25	30	28	5	5	5	5	38
20	22C11A0481	LINGAM SRAVANI	21	26	24	5	5	5	5	34
21	22C11A0482	BODDU SREEJA	24	28	26	5	5	5	5	36

22	22C11A0483	EATUKURI SRI LAKSHMI	30	30	30	5	5	5	5	40
23	22C11A0484	KAVURI SRICHANDANA	22	27	25	5	5	5	5	35
24	22C11A0485	KUKKALA SRUJAN	19	17	18	5	5	5	5	28
25	22C11A0486	RAVELLA SURYA	13	15	14	5	5	5	5	24
26	22C11A0487	KUNCHALA TRIVENI	25	29	27	5	5	5	5	37
27	22C11A0488	PEDANATI UDAY SAINADH	15	AB	8	0	0	0	0	8
28	22C11A0489	SIRAM SETTI UMAMAHESH	24	30	27	5	5	5	5	37
29	22C11A0490	BANOTHU USHA	25	27	26	5	5	5	5	36
30	22C11A0491	DHANIYAKULA USHASRI	21	27	24	5	5	5	5	34
31	22C11A0492	ATHKURI VAMSHI	24	25	25	5	5	5	5	35
32	22C11A0493	THAMMINENI VENNELA	12	19	16	5	5	5	5	26
33	22C11A0494	PALLA VIJAY KUMAR	AB	AB	0	0	0	0	0	0
34	22C11A0495	GUNNAM VIJAY SIMHA REDDY	25	18	22	5	5	5	5	32
35	22C11A0496	KASANI VINAY TEJA	21	24	23	5	5	5	5	33
36	22C11A0497	TELAGORLA VINAY	20	20	20	5	5	5	5	30
37	22C11A0498	DAMMALAPATI VINOD KUMAR	22	20	21	5	5	5	5	31
38	22C11A0499	KATIKAM VISHVA TEJA	12	16	14	5	5	5	5	24
39	22C11A04A0	BANOTHU YAMINI NAIK	18	25	22	5	5	5	5	32
40	22C11A04A1	BASANAKARRA YASHWANTH	22	21	22	5	5	5	5	32
41	22C11A04A2	REMIDALA YASHWANTH	18	15	17	5	5	5	5	27
42	22C11A04A3	SAYYAD YASIN	14	14	14	5	5	5	5	24
43	22C11A04A4	MACHIREDDY PRATHYUSHA	26	29	28	5	5	5	5	38
44	22C11A04A5	REDDIMALLA BHANU PRAKASH	17	19	18	5	5	5	5	28
45	23C15A0401	AKHILESHWARI SUDDALA	22	24	23	5	5	5	5	33
46	23C15A0402	ANJALICHILAKAM ARRI	20	29	25	5	5	5	5	35
47	23C15A0403	DURGA SAI ACHANTA	24	28	26	5	5	5	5	36
48	23C15A0404	HARINI SHANAGAPATI	26	30	28	5	5	5	5	38

49	23C15A0405	LAXMI GAYATHRI NERELLA	24	30	27	5	5	5	5	37
50	23C15A0406	MUKESH SIVAKAVI	18	17	18	5	5	5	5	28
51	23C15A0407	NAVYA SRI MADURI	25	26	26	5	5	5	5	36
52	23C15A0408	RAMARAO THODETI	24	24	24	5	5	5	5	34
53	23C15A0409	SAMAD SHAIK	27	26	27	5	5	5	5	37
54	23C15A0410	SANDEEP ATHMAKURU	28	30	29	5	5	5	5	39
55	23C15A0411	VENKATA KRISHNA KARAMSETTI	22	26	24	5	5	5	5	34