Question Paper Code: R18A41EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

IV B.Tech I Semester Regular/Supplementary Examinations, Dec-2024

VLSI DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions

		Course Outcome	B.T Level	Marks
1.	MOSFETs are said to be more efficient than BJTs. Justify the answer.	CO1	L2	2M
2.	Explain Latch-up.	CO1	L2	3M
3.	What are the limitations of scaling?	CO2	L1	2M
4.	Define feature size and state the objectives of layout design rules.	CO2	L1	3M
5.	Define switch logic?	CO3	L1	2M
6.	List out the types of alternative gate circuits.	CO3	L1	3M
7.	What is memory array subsystem?	CO4	L1	2M
8.	What are Programmable Interconnects?	CO4	L1	3M
9.	What are bit wise operators in Verilog?	CO5	L1	2M
10.	Mention the four key words used in Verilog.	CO5	L1	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Explain analytically the behaviour of a CMOS inverter with its transfer characteristics.	CO1	L2	10M
	OR			
B)	Explain different forms of pull-ups used as load in CMOS enhancement and prove Zpu/Zpd = 4/1.	CO1	L2	10M
12. A)	Write a short note on Lambda based design rules.	CO2	L3	10M
	OR			
B)	Draw the schematic and stick diagram of 2 input CMOS NAND gate.	CO2	L3	10M
13. A)	What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors.	CO3	L2	10M
	OR			
B)	Define fan-in and fan-out. Explain their effects on propagation delay.	CO3	L3	10M
14. A)	Show the logic diagram of zero/one detector & explicate its operation with help of diagram.	CO4	L2	10M
	OR			
B)	Draw and explain the routing architecture of field programmable gate arrays.	CO4	L3	10M
15. A)	Explain the concept involved in Timing control in VERILOG.	CO5	L2	10M
	OR			
B)	Write a Verilog code for binary to gray code convertor.	CO5	L2	10M