Question Paper Code: R18A21EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech. I Semester Supplementary Examinations, December – 2024

DIGITAL LOGIC DESIGN

(COMPUTER SCIENCE AND ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions	Course Outcome	B.T Level	Marks
1. Convert the binary number 101101 to its decimal, octal, and hexadecimal equivalents.	CO1	L2	2M
2. Define floating-point representation. Why is it used in computer systems?	CO1	L1	3M
3. What is a Karnaugh Map (K-Map), and how is it used for gate minimization?	CO2	L1	2M
4. Explain the relationship between NAND and NOR gates as universal gates.	CO2	L2	3M
5. Define combinational circuits and give examples.	CO3	L1	2M
6. Explain the process of binary-to-BCD conversion.	CO3	L2	3M
7. What is state reduction? Why is it important in the design of sequential circuits?	CO4	L1	2M
8. Explain the working of an SR latch and its application in sequential circuits.	CO4	L2	3M
9. What is the difference between associative memory and auxiliary memory?	CO5	L1	2M
10. Describe the process of expanding a memory system using small memories and decoders.	CO5	L2	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Generate a Hamming code for the data sequence 1011 and demonstrate how a single-bit error is detected and corrected.	CO1	L3	10M
	OR			
B)	Perform the following operations using 1's and 2's complement methods: i) 1101_2-1001_2 ii) 0110_2-1110_2 iii) 0101_2-1010_2	CO1	L3	10M
12. A)	Using a 4-variable K-Map, simplify the Boolean function $F(W,X,Y,Z)=\Sigma m(1,3,7,11,15)+d(0,2,5,8)$.	CO2	L3	10M
	OR			
B)	Design an 8-to-3 encoder and provide its truth table and Boolean equations.	CO2	L3	10M
13. A)	Design a half adder and a full adder. Include truth tables, Boolean equations, and circuit diagrams.	CO3	L3	10M
	OR			
B)	Simplify the full adder equations and implement the circuit using only XOR gates and a single OR gate.	CO3	L3	10M

14. A)	Design a 4-bit synchronous counter using JK flip-flops and explain the operation.	CO4	L3	10M
	OR			
B)	Design a BCD counter using synchronous flip-flops. Show the state diagram, state table, and transition logic.	CO4	L3	10M
15. A)	Compare and contrast different types of ROM. Include their programming methods and uses.	CO5	L2	10M
	OR			
B)	Design a memory system with 256 words, where each word is 16 bits. Using a 4-to-16 decoder, explain how you would select a specific memory word.	CO5	L3	10M