Question Paper Code: R18A21EC03

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Supplementary Examinations, December–2024

SWITCHING THEORY AND LOGIC DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (10 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	State the use of codes in digital electronic systems?	CO1	L1	2M
2.	Convert decimal 13.7 to a binary number?	CO1	L2	3M
3.	What is Karnaugh map?	CO2	L1	2M
4.	What are the applications of multiplexes?	CO2	L1	3M
5.	Explain the operation of D-latch flip flop?	CO3	L2	2M
6.	Define Flip-flop?	CO3	L1	3M
7.	Draw the shift Registers?	CO4	L2	2M
8.	Summarize the state Reduction and state diagram?	CO4	L2	3M
9.	What are the limitations of a finite-state machine?	CO5	L1	2M
10.	Name conventional flow chart and ASM chart blocks?	CO5	L2	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Briefly explain errors detecting and errors correcting codes with examples?	CO1	L3	10M
	OR			
B)	List the theorems of Boolean Algebra and prove them?	CO1	L3	10M
12. A)	Briefly explain the operation of a multiplexer?	CO2	L3	10M
	OR			
B)	Explain the significance of Truth tables and k-maps?	CO2	L3	10M
13. A)	How do you convert an RS flip flop into T flip flop?	CO3	L3	10M
	OR			
B)	Draw and explain its operation of JK master slave flip-flop systems?	CO3	L3	10M
14. A)	Discuss the Realization using flip-flop counters?	CO4	L3	10M
	OR			
B)	Explain the Ring counter using shift register?	CO4	L3	10M
15. A)	Distinguish between Mealy and Moore machines?	CO5	L3	10M
	OR			
B)	Explain the construction of ASM chart?	CO5	L3	10M