

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech II Semester Supplementary Examinations, December – 2024

SWITCHING THEORY AND LOGIC DESIGN

(ELECTRICAL AND ELECTRONICS ENGINEERING)

Time: 3 Hours**Max. Marks: 75****Section – A (Short Answer type questions)****(25 Marks)****Answer All Questions**

	Course Outcome	B.T Level	Marks
1. Find 2's complement of $(10100011)_2$	CO1	L1	2M
2. Give the classification of binary codes.	CO1	L1	3M
3. Implement the given expression using logic gates $F=AB+CD'+B'C$	CO2	L2	2M
4. Simplify using k-map $F(A, B, C)=\sum m(0,1,2,3,4,5,6,7)$.	CO2	L2	3M
5. Give the comparison between combinational and sequential circuits	CO3	L2	2M
6. Convert JK flip flop to T flip flop.	CO3	L2	3M
7. Define state diagram and state table.	CO4	L1	2M
8. Distinguish Moore and Mealy FSMs.	CO4	L2	3M
9. What is Merger chart?	CO5	L1	2M
10. Mention the limitations of FSM.	CO5	L1	3M

Section B (Essay Questions)**Answer all questions, each question carries equal marks.****(5 X 10M = 50M)**

11. A) Convert the following binary numbers to Decimal, Hexadecimal and octal forms i) $(101101.1101)_2$ ii) $(11011011.100101)_2$	CO1	L3	10M
OR			
B) Implement the following using NAND-NAND realization. i) $AC+ABC+A'BC+AB+D$ ii) $F=A'B'+A'C+B'C$	CO1	L3	10M
12. A) Draw and explain 4-Bit comparator.	CO2	L3	10M
OR			
B) Draw and explain 16 to 1 multiplexer.	CO2	L3	10M
13. A) What is racing problem and explain how it is overcome in JK flip flop.	CO3	L3	10M
OR			
B) What is excitation table with the excitation tables explain the operation of JK, RS, D and T flip flops.	CO3	L3	10M
14. A) Explain clearly design aspects of synchronous sequential FSMs.	CO4	L2	10M
OR			
B) Design and explain clearly the procedure of single mode counter.	CO4	L2	10M
15. A) Draw and explain clearly about weighing machine with a neat flow chart.	CO5	L2	10M
OR			
B) Explain clearly data path subsystem for binary Multiplier.	CO5	L3	10M