Question Paper Code: R18A31EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

III B.Tech I Semester Supplementary Examinations, December-2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions

		Course Outcome	B.T Level	Marks
1.	Draw the basic block diagram of a computer.	CO1	L1	2M
2.	Define addressing mode.	CO1	L1	3M
3.	Define interrupt.	CO2	L1	2M
4.	Define stack.	CO2	L1	3M
5.	Define micro instruction.	CO3	L1	2M
6.	What is the use of mapping.	CO3	L2	3M
7.	What is the use of cache memory.	CO4	L2	2M
8.	Define virtual memory.	CO4	L1	3M
9.	Expand USB.	CO5	L1	2M
10.	Define hand shaking.	CO5	L1	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Write the differences between Von-Neumann model and Harvard model with block diagrams.	CO1	L2	10M
	OR			
B)	Describe different addressing modes used in computer architecture.	CO1	L3	10M
12. A)	Write short notes on instruction cycle.	CO2	L3	10M
	OR			
B)	Write the differences between memory based and register based addressing modes.	CO2	L3	10M
13. A)	Discuss about micro programmed control organization with a neat diagram.	CO3	L3	10M
	OR			
B)	Write short notes on address sequencing.	CO3	L3	10M
14. A)	Describe the different types of ROM and explain them.	CO4	L3	10M
	OR			
B)	Describe how to design a combinational circuit with memory.	CO4	L3	10M
15. A)	Write short notes on asynchronous data transfer mode.	CO5	L2	10M
	OR			
B)	Briefly explain the operation of RS232.	CO5	L2	10M