Question Paper Code: R22A21CS03

R22

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Regular/Supplementary Examinations, December – 2024

COMPUTER ORGANIZATION AND ARCHITECTRE

(COMMON TO CSE & AIML)

Time: 3 Hours **Max. Marks: 60**

Section – A (Short Answer type questions) (10 Marks)

Answer All Questions

		Course Outcome	B.T Level	Marks
1.	What is the purpose of register?	CO1	L1	1M
2.	What is a Micro Operation?	CO1	L1	1M
3.	What is the meaning of program control?	CO2	L1	1M
4.	Give an example for micro instruction.	CO2	L1	1M
5.	What is arithmetic with decimals?	CO3	L1	1M
6.	What are the different types of data in digital computer?	CO3	L1	1M
7.	What is the purpose of cache memory?	CO4	L1	1M
8.	What is priority interrupt?	CO4	L1	1M
9.	State the stages of instruction pipeline.	CO5	L1	1M
10.	What are the different types of array processors?	CO5	L1	1M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Explain arithmetic, logic and shift micro-operations with example.	CO1	L2	10M
	OR			
B)	What is instruction cycle? Explain various steps involved in the instruction cycle.	CO1	L2	10M
12. A)	With the diagram explain the basic organization of micro programmed control unit.	CO2	L2	10M
	OR			
B)	What is meant by addressing? Explain the various common addressing modes with examples and illustrations	CO2	L2	10M
13. A)	Demonstrate the booth multiplication algorithm in detail with diagram.	CO3	L3	10M
	OR			
B)	Explain with examples how the floating-point numbers are represented and used in digital arithmetic operations. Give an example.	CO3	L2	10M
14. A)	Draw the block diagram of DMA controller and explain its functioning.	CO4	L3	10M
	OR			
B)	Elaborate in detail the memory hierarchy with neat diagram.	CO4	L3	10M
15. A)	Demonstrate the two-stage instruction pipeline with neat diagram illustration.	CO5	L3	10M
	OR			
B)	Explain the concept of cache coherence problem and its solution.	CO5	L2	10M