ANURAG Engineering College

(An Autonomous Institution)

II B.Tech II Semester Supplementary Examinations, December – 2024 LINEAR AND DIGITAL ICAPPLICATIONS (ELECTRONICS & COMMUNICATION ENGINEERING)

Time: 3 Hours Max. Marks: 60

Time.	3 Hours	171	aa. waa	W2. OA
Section – A (Short Answer type questions) Answer All Questions		Course	(10 B.T Level	Marks) Marks
1.	Draw a typical gain versus frequency graph for an operational amplifier	Outcome CO1	Level L1	1M
2.	Evaluate the common mode gain if the CMRR is 80 dB and the differential mode gain is 60dB.	CO1	L2	1M
3.		CO2	L2	1M
4.	Design a first -order active LPF to have a cut off frequency of 5 kHz.	CO2	L3	1M
5.	Mention the drawbacks of binary-weighted type ADC.	CO3	L1	1M
6.	Write the equation for output analog voltage for a generalized DAC.	CO3	L1	1M
7.	Give the comparison between TTL and CMOS logic families.	CO4	L2	1M
8.	Draw the circuit diagram of 74LS151.	CO4	L1	1M
	Draw the circuit diagram for decade counter.	CO5	L1	1M
10.	Draw the basic architecture of 1 KB SRAM.	CO5	L1	1M
	Section B (Essay Questions)			
Answe	r all questions, each question carries equal marks.	(5	X 10M	=50M)
11. A)	i) Draw the circuit diagram and briefly explain the operation of instrumentation amplifier.	CO1	L2	5M
	ii) Draw and explain the block diagram of IC723. OR	CO1	L2	5M
B)	i) Design a practical integrator circuit to properly process input sinusoidal waveforms up to 1KHz. The input amplitude is 10mV.	CO1	L3	5M
	ii) Draw and explain the operation of Schmitt Trigger with neat waveforms.	CO1	L2	5M
12. A)	i) Design an op-amp based astable multivibrator to generate a square waveform of frequency 2 KHz. (Make necessary assumptions.)	CO2	L3	5M
	ii) Draw the diagram of PLL and explain its operation. OR	CO2	L2	5M
B)	i) Design a BPF with Lower cut-off frequency of 2 KHz and upper cutoff frequency of 5 KHz using IC 741.	CO2	L3	5M
	ii) Write the operation of mono stable multi vibrator using op-amp and derive the expression to calculate the time delay produced by it.	CO2	L2	-5M
13. A)	i) Explain the working of 3-bit D to A converter using R-2R ladder network.	CO3	L2	5M
	ii) Discuss in detail the operation of successive approximation type ADC. Mention its advantages	CO3	L2	5M
	OP			

B)	i) Discuss about the importance of Analog to Digital and Digital to Analog Conversion.	CO3	L2	5M
	ii) Draw and explain the working of binary weighted resistor type DAC.	CO3	L2	5M
14. A)	i) Draw and explain the operation of (IC 74LS138) 3x8 decoder.	CO4	L2	5M
•	ii) Design an 8 x 1 multiplexer using 4 x 1 multiplexers. OR	CO4	L3	5M
B)	i) Design and analyze a BCD to Excess-3 code converter.	CO4	L3	5M
	ii) Draw and explain the operation of (IC 74LS348) priority encoder.	CO4	L2	5M
15. A)	i) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams.	CO5	L2	5M
	ii) Draw and explain the architecture of ROM.	CO5	L2	5M
	OR			
B)	i) Design a 4-bit universal shift register and explain its working in detail.	CO5	L3	5M
	ii) Give the comparison of RAM an ROM.	CO5	L2	5M