Question Paper Code: R18A21EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Supplementary Examinations, Jan/Feb-2024

DIGITAL LOGIC DESIGN

(COMPUTER SCIENCE AND ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Marks	CO	B.T. Level
1.	What is the largest binary number that can be expressed with 12 bits? What is the equivalent decimal ?	2M	CO1	L1
2.	Express -73.75 in 2's complement form.	3M	CO1	L2
3.	Convert the following Boolean function to Canonical form. $F = \bar{A}B + BC + D$	2M	CO2	L2
4.	Define Encoder. And how does an encoder differ from decoder.	3M	CO2	L1
5.	Explain Half Adder.	2M	CO3	L1
6.	Draw the circuit diagram of 4-bit parallel adder/subtractor.	3M	CO3	L2
7.	Write the difference between combinational circuit and sequential circuit.	2M	CO4	L1
8.	Explain SR flip flop with the excitation table.	3M	CO4	L2
9.	What is ROM? Explain Types of ROMs.	2M	CO5	L1
10.	Write the comparison between RAM and ROM.	3M	CO5	L2

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50 M)**

11.	A)	Convert the following number systems. i) $(1011101.0101)_2$ to Octal number ii) $(CB289.36)_{16}$ to Decimal number iii) $(54)_6$ to Binary number iv) $(275)_8$ to Hexadecimal number v) $(4310)_5$ to Decimal number	10M	CO1	L3
		OR			
	B)	i) What is a Hamming code and encode data bits 10110 into a 8-bit odd parity Hamming code.	5M	CO1	L3
		ii) Explain about Weighted and Non-weighted codes.	5M		
12.	A)	Minimize the following Boolean expressions using K-Map i) f1 = Σm (5, 7, 8, 10, 13, 15) + d (0, 1, 2, 3) ii) f2 = ΠM (1, 2, 6, 7, 8, 13, 14, 15).	10M	CO2	L3
		OR			
	B)	Implement a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to- 4-line decoder.	10M	CO2	L3
13.	A)	Design and implement full subtractor by using only NAND gates. Explain its operation with the help of truth table?	10M	CO3	L3
		OR			
	B)	Design the full adder circuit using decoder and de-multiplexer.	10M	CO3	L3

14.	A)	What is difference between latch and flip flop? Explain about clocked JK flip flop using NAND gates.	10M	CO4	L2
		OR			
	B)	Design a synchronous BCD counter with JK flip-flop.	10M	CO4	L3
15.	A)	Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM.	10M	CO5	L3
		OR			
	B)	Discuss on the concepts and applications of ROM, PROM and EPROM.	10M	CO5	L2