Question Paper Code: R18A21EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech. I Semester Supplementary Examinations, June/July – 2024

DIGITAL LOGIC DESIGN

(COMPUTER SCIENCE AND ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Convert 1234 Base 8 to Base 2 (binary)	CO1	L1	2M
2.	Explain the representation of single precision and double precision floating point?	CO1	L3	3M
3.	What is the need for don't cares in K maps?	CO2	L4	2M
4.	Explain the canonical and standard forms?	CO2	L3	3M
5.	What is a combinational circuit?	CO3	L2	2M
6.	Explain about 4-bit binary parallel adder.	CO3	L1	3M
7.	How many bits we can store using a flip flop?	CO4	L1	2M
8.	Explain about ripple counter?	CO4	L3	3M
9.	List out the various types of ROM?	CO5	L3	2M
10.	List out the difference Associative and Auxiliary memory	CO5	L2	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. (5 X 10M = 50M)

11. A)	i) Apply 2's complement subtraction for the binary numbers 101100 – 110110. ii) Explain about even parity and odd parity?	CO1	L2	
	OR			
B)	Demonstrate about the error correction and error detection capabilities of hamming code with an example.	CO1	L3	10M
12. A)	Minimize the following boolean function using K-map $F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$	CO2	L2	10M
	OR			
B)	Analyze 4*16 decoder with 2*4 decoders.	CO2	L3	10M
13. A)	Construct and analyze half adder and full adder operations with neat diagram.	CO3	L2	10M
	OR			
B)	Sketch the k-map for BCD to GRAY CODE and design the logic diagram.	CO3	L3	10M
14. A)	Examine the working principle of JK & T flip-flops truth tables.	CO4	L2	10M
	OR			
B)	Design a synchronous counter for the sequence: $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$, using J-K flip-flop.	CO4	L2	10M
15. A)	Design of 512×8 RAM using 128×8 RAM.	CO5	L3	10M
	OR			
B)	Explain the cache memory and its design issues.	CO5	L3	10M