Question Paper Code: R22A22CS02

R18

# ANURAG Engineering College

## (An Autonomous Institution)

## II B.Tech II Semester Supplementary Examinations, Jan/Feb2024

## COMPUTER ORGANIZATION

## (COMPUTER SCIENCE AND ENGINEERING)

**Time: 3 Hours** **Max. Marks: 75**

### Section – A (Short Answer type questions) (25 Marks)

| Answer All Questions | | Course Outcome | B.T Level | Marks |
|---|---|---|---|---|
| 1. | Define computer organization. | CO1 | L1 | 2M |
| 2. | List the characteristics of CISC. | CO1 | L1 | 3M |
| 3. | State the major characteristics of pipeline. | CO2 | L1 | 2M |
| 4. | Differentiate serial and parallel processing. | CO2 | L2 | 3M |
| 5. | Differentiate main memory and auxiliary memory. | CO3 | L2 | 2M |
| 6. | Why memory hierarchy is important in computer system? | CO3 | L2 | 3M |
| 7. | Write down the function of I/O module. | CO4 | L2 | 2M |
| 8. | How Asynchronous data transfer occurs? | CO4 | L2 | 3M |
| 9. | State the features of crossbar switch. | CO5 | L1 | 2M |
| 10. | How many ports does a multiport memory have? | CO5 | L2 | 3M |

### Section B (Essay Questions)

**Answer all questions, each question carries equal marks.** **(5 X 10M = 50M)**

| | | | | |
|---|---|---|---|---|
| 11. A) | Summarize the significance of addressing modes and explain how to calculate effective address in each addressing mode with an example. | CO1 | L3 | 10M |
| | **OR** | | | |
| B) | Explain in detail about Instruction cycle state diagram. | CO1 | L2 | 10M |
| 12. A) | Explain about Delayed load and Delayed branch | CO2 | L2 | 10M |
| | **OR** | | | |
| B) | What is pipe lining? Demonstrate six stages of CPU instruction pipeline | CO2 | L3 | 10M |
| 13. A) | What is the need of replacement algorithm for a cache memory? Explain any two cache replacement strategies. | CO3 | L3 | 10M |
| | **OR** | | | |
| B) | Explain address sequencing mechanism in micro programmed control | CO3 | L2 | 10M |
| 14. A) | What do you understand by the term'program Interrupt'? Explain with the help of suitable diagrams. | CO4 | L3 | 10M |
| | **OR** | | | |
| B) | Illustrate the series of actions that a DMA controller will perform after it receives a request from a peripheral device to transfer data from the peripheral device to memory. | CO4 | L3 | 10M |
| 15. A) | Illustrate with necessary example, the memory organization in multiprocessor. | CO5 | L3 | 10M |
| | **OR** | | | |
| B) | Explain Flynn's classifications with suitable diagrams. | CO5 | L2 | 10M |