Question Paper Code: R18A22EC05

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech II Semester Supplementary Examinations, Jan/Feb-2024

SWITCHING THEORY AND LOGIC DESIGN

(ELECTRICAL AND ELECTRONICS ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Convert 615 octal to its hexadecimal equivalent.	CO1	L1	2M
2.	Mention demorgan's theorems.	CO1	L2	3M
3.	Define full and half subtractors.	CO2	L1	2M
4.	Define multiplexer.	CO2	L1	3M
5.	What is triggering and mention types of triggering.	CO3	L2	2M
6.	Define clock skew.	CO3	L1	3M
7.	Define state table and state diagram.	CO4	L1	2M
8.	Define modules of a counter.	CO4	L2	3M
9.	What is mealy machine.	CO5	L2	2M
10.	Mention any two/three salient features of ASM chart.	CO5	L1	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Convert the given expression into standard POS form Y=A.(A+B+C)	CO1	L3	10M
	OR			
B)	Realize XOR and XNOR gates using NAND only and NOR only gates.	CO1	L3	10M
12. A)	Simplify the following Boolean function by using Quine-Mccluskey method. $F(A,B,C,D)=\sum m(0,2,3,6,7,8,10,12,13)$	CO2	L3	10M
	OR			
B)	Design full adder and full subtractor circuits.	CO2	L3	10M
13. A)	Draw and explain +ve edge triggered D-flip flop and JK flip flop.	CO3	L3	10M
	OR			
B)	Convert JK flip flop to D, D flip flop to T, T flip flop to D.	CO3	L3	10M
14. A)	Design 4-bit shift register to perform shift left and shift right operations.	CO4	L3	10M
	OR			
B)	Design 4-bit ripple counter to perform up count and down count.	CO4	L3	10M
15. A)	Discuss partition techniques and merger chart methods.	CO5	L3	10M
	OR			
B)	Design binary Multiplier.	CO5	L3	10M