Question Paper Code: R18A22EC07

R18

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech II Semester Supplementary Examinations, June/July – 2024

SWITCHING THEORY AND LOGIC DESIGN

(ELECTRICAL AND ELECTRONICS ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Find the decimal digits 0-9 in BCD code and 2 4 2 1 code.	CO1	L1	2M
2.	Show that the dual of the Exclusive – OR is equal to its complement	CO1	L2	3M
3.	Make use of the Boolean function F(X,Y,Z)=∑m(3,4,6,7) using K-map.	CO2	L1	2M
4.	Define a MUX and show how a MUX may be used as a sequence data selector.	CO2	L2	3M
5.	Compare Latch and Flip-Flop.	CO3	L1	2M
6.	Define Level trigger, Edge trigger, Clock skew.	CO3	L2	3M
7.	Compare asynchronous and synchronous counters.	CO4	L1	2M
8.	What are the drawbacks of ripple counters.	CO4	L2	3M
9.	List the capabilities of finite state machine.	CO5	L1	2M
10.	Explain about partition techniques.	CO5	L2	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	What is a reflected code? Write about reflected codes by giving examples.	CO1	L2	10M
	OR			
B)	Construct BCD code to Gray code converter with diagram.	CO1	L3	10M
12. A)	Simplified expressions in sum of products for the following Boolean functions using Karnaugh-Map. i) F(A, B,C,D) = Σ (7,13, 14, 15) ii) F(w,x,y,z) = Σ (2,3,12,13,14,15)	CO2	L2	10M
	OR			
B)	Simplify the following function using Tabular method f(w,x,y,z)= ∑m(4,5,6,7,12,13,14)+ ∑d(1,9,11,15)	CO2	L3	10M
13. A)	Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.	CO3	L2	10M
	OR			
B)	Write the conversion procedures of the flip-flops. Convert T-flip-flop to JK- flip-flop.	CO3	L2	10M
14. A)	Construct the state diagram for a two input, two output sequential circuit which is to produce an output z=1 with occurrence of an input 1 following a string of two or three consecutive input 0's. At all other times the output is to be 0, realize using JK flipflop.	CO4	L3	10M
	OR			
B)	Develop and explain a synchronous MOD-12 down-counter using J-K flipflop.	CO4	L2	10M

15. A)	Explain the procedure of state minimization using the partition technique.	CO5	L3	10M
	OR			
B)	Analyze the ASM chart for Binary multiplier with an example.	CO5	L3	10M