Question Paper Code: R18A31EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

III B.Tech I Semester Regular/Supplementary Examinations, Dec–2023/Jan-2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max.Marks:75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Define ROM and RAM	CO1	L1	2M
2.	What are the registers involved in fetching an instruction from memory to processor?	CO1	L1	3M
3.	List the types of interrupts	CO2	L1	2M
4.	What is the transfer register?	CO2	L1	3M
5.	Differentiate control memory and main memory	CO3	L2	2M
6.	What is micro programming?	CO3	L1	3M
7.	Define virtual memory	CO4	L1	2M
8.	Why the access time of the cache memory is lesser than the access time of the main memory	CO4	L2	3M
9.	List the functions of input-output interface	CO5	L1	2M
10.	What is the IEEE 1394 protocol?	CO5	L1	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. (5 x 10M = 50M)

11. A)	What are the different types of computer instructions? Explain how they are differentiated	CO1	L2	10M
	OR			
B)	Define CISC and RISC and compare any four features of CISC and RISC	CO1	L2	10M
12. A)	List and explain various shift micro operations in detail with 4 bit circuit shifter diagram.	CO2	L2	10M
	OR			
B)	Write push and pop operations for register stack organization.	CO2	L3	10M
13. A)	Demonstrate about address sequencing with neat diagram	CO3	L3	10M
	OR			
B)	Explain the working of a hardwired control unit with a suitable diagram	CO3	L2	10M
14. A)	Write about associative mapping and direct mapping in cache memory	CO4	L3	10M
	OR			
B)	Discuss about the virtual memory? Discuss about the mapping of virtual address to memory table	CO4	L2	10M
15. A)	With a neat sketch explain the working principle of DMA	CO5	L3	10M
	OR			
B)	Explain different priority interrupts in detail	CO5	L2	10M