Question Paper Code: R18A31EC04

R18

ANURAG Engineering College

(An Autonomous Institution)

III B.Tech I Semester Supplementary Examinations, June/July - 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(ELECTROICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Differentiate between SRAM & DRAM.	CO1	L2	2M
2.	How many registers are there in SIC XE?	CO1	L1	3M
3.	List any four addressing modes where effective address is obtained by computation.	CO2	L1	2M
4.	What do you mean by an interrupt?	CO2	L1	3M
5.	What is control memory?	CO3	L1	2M
6.	What are the different types of control units?	CO3	L1	3M
7.	What are the different types of secondary storage?	CO4	L1	2M
8.	What is read-only memory and its types?	CO4	L1	3M
9.	What are the different types of data transfer mode?	CO5	L1	2M
10.	What is the advantage of data transfer using DMA?	CO5	L1	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Compare the key features of CISC and RISC architectures.	CO1	L2	10M
	OR			
B)	Demonstrate the Von Neumann architecture	CO1	L3	10M
12. A)	Explain various phases of the instruction cycle in detail using neat sketches.	CO2	L2	10M
	OR			
B)	What is an addressing mode? Explain various addressing modes with examples.	CO2	L2	10M
13. A)	Explain about micro programmed control with neat sketch.	CO3	L2	10M
	OR			
B)	Draw the hardwired control unit organization and explain the functionality of each block	CO3	L3	10M
14. A)	Explain cache mapping functions with examples.	CO4	L2	10M
	OR			
B)	What is virtual memory? Discuss how paging helps in implementing virtual memory	CO4	L3	10M
15. A)	What is interrupt? Explain the priority interrupt technique	CO5	L2	10M
	OR			
B)	Explain the method of DMA transfer. How does a DMA controller improve the performance of a computer?	CO5	L3	10M