Question Paper Code: R18A41EC01

R18

ANURAG Engineering College

(An Autonomous Institution)

IV B.Tech I Semester Supplementary Examinations, April – 2024

VLSI DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max. Marks: 75**

Section – A (Short Answer type questions) (25 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	Draw symbols of nmos, pmos and cmos transistors.	CO1	L1	2M
2.	Define oxidation, diffusion and implantation.	CO1	L1	3M
3.	Mention MOS layers.	CO2	L2	2M
4.	Give scaling factors for gate Area, channel resistance and gate capacitance.	CO2	L2	3M
5.	Define sheet resistance.	CO3	L1	2M
6.	Draw pseudo nmos 2-input Nand gate.	CO3	L2	3M
7.	Define FPGA.	CO4	L1	2M
8.	Distinguish PLA and PAL.	CO4	L3	3M
9.	Give syntax of entity declaration.	CO5	L1	2M
10.	Write program for 2-input OR gate in Verilog.	CO5	L2	3M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	With neat sketches explain fabrication process of p-well CMOS transistor.	CO1	L2	10M
	OR			
B)	Derive I_{ds} versuss V_{ds} relationship for nmos enhancement regions.	CO1	L2	10M
12. A)	Explain in detail about VLSI design flow with neat diagram.	CO2	L2	10M
	OR			
B)	Explain scaling factors and limitations on scaling.	CO2	L2	10M
13. A)	Draw dynamic CMOS 3-input NAND and NOR gates.	CO3	L3	10M
	OR			
B)	Discuss in detail about various basic circuit concepts.	CO3	L3	10M
14. A)	Draw and explain FPGA architecture.	CO4	L3	10M
	OR			
B)	Discuss serial parallel multiplier and comparators.	CO4	L2	10M
15. A)	Write Verilog program for 3 to 8 Decoder.	CO5	L3	10M
	OR			
B)	Write Verilog program for 8 to 1 multiplexer.	CO5	L3	10M