## **ANURAG Engineering College**

(An Autonomous Institution)

II B. Tech. I Semester Supplementary Examinations, June/July – 2024 ELECTRONIC DEVICES AND CIRCUITS (COMMON TO (R18-EEE, ECE & CSE) & (R15-CSE))

Time: 3 Hours Max.Marks:75 Section – A (Short Answer type questions) (25 Marks) Marks **Answer All Questions** Course B.T Outcome Level 1. Draw the Piece-wise linear approximation model of the diode with CO<sub>1</sub> L1 2M relevant V-I graph. 2. Discuss Avalanche breakdown mechanism. CO<sub>1</sub> L2 3M 3. Define faithful amplification. L1 CO<sub>2</sub> 2M 4. Draw the symbols of BJT, FET and MOSFET. CO<sub>2</sub> L1 3M 5. What is meant by Operating Point? CO<sub>3</sub> L2 2M 6. Write the need for biasing in Transistors. CO<sub>3</sub> L1 3M 7. Define Intrinsic stand-off ratio. CO<sub>4</sub> L1 2M 8. Mention the advantages and limitations of FET over BJT. CO<sub>4</sub> L1 3M 9. What are the feedback used in amplifiers, and oscillators? CO<sub>5</sub> L1 2M10. Discuss Barkhausen Criterion. CO<sub>5</sub> L2 3M Section B (Essay Questions) Answer all questions, each question carries equal marks.  $(5 \times 10M = 50M)$ 11. A) Explain the behavior of PN-junction diode under forward, and CO<sub>1</sub> L3 10M reverse biased conditions with the help of neat diagrams and graphs. OR B) What is the role of filter circuit in a Rectifier? List and compare the L3 CO<sub>1</sub> 10M working principles of different filters that are used in Rectifiers. 12. A) Discuss the working principle and the operation of NPN transistor CO<sub>2</sub> L3 10M with diagrams and graphs. OR B) Explain in detail the construction and principle of operation of n-CO<sub>2</sub> L3 10M channel JFET with neat diagrams and graphs. Analyze the working of Fixed Bias, Collector Feedback Bias, CO<sub>3</sub> L3 10M Emitter Feedback Bias, Voltage Divider Bias circuits in eliminating thermal runaway. B) Discuss in detail Stabilization against variation in I<sub>CO</sub>, V<sub>BE</sub> and β. CO<sub>3</sub> L3 10M 14. A) Analyse a transistor amplifier circuit using h-parameter model and CO<sub>4</sub> L3 10M evaluate Current gain, Voltage gain, Input resistance, and Output admittances for CE configuration. B) Explain the operation of UJT with neat diagrams and V-I CO<sub>4</sub> L3 10M characteristics.

Draw the circuit diagram of voltage series feedback amplifier and

derive expressions for gain, input resistance and output resistance.

B) Explain Hartley oscillator with necessary derivations and diagrams.

10M

10M

L3

L3

CO<sub>5</sub>

CO<sub>5</sub>