Question Paper Code: R22A21CS03

R22

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Regular Examinations, Jan/Feb–2024

COMPUTER ORGANIZATION AND ARCHITECTRE

(COMMON TO CSE & AIML)

Time: 3 Hours **Max. Marks: 60**

Section – A (Short Answer type questions) (10 Marks)

Answer All Questions		Course Outcome	B.T Level	Marks
1.	What is Register Transfer Language?	CO1	L1	1M
2.	Name any three register reference instructions	CO1	L1	1M
3.	What is the difference between hard wired control unit and microprogrammed control unit.	CO2	L1	1M
4.	What are the different types of instruction formats according to the number of addresses present in the instruction.	CO2	L1	1M
5.	Show $-35_{(10)}$ in Signed 2'complement representation.	CO3	L1	1M
6.	What is IEEE floating point representation.	CO3	L1	1M
7.	Define Direct Memory Access data transfer.	CO4	L1	1M
8.	What is Associative Memory?	CO4	L1	1M
9.	List any 2 characteristics of RISC system.	CO5	L1	1M
10.	What is the purpose of Array processor.	CO5	L1	1M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	(i) Explain all the logical microoperations with neat diagram.	CO1	L2	5M
	(ii) Summarize any three memory reference instructions and explain in detail.	CO1	L2	5M
	OR			
B)	Explain the Instruction cycle by drawing neat flowchart.	CO1	L2	10M
12. A)	Compare Hardwired control unit and Microprogrammed control unit and explain Address sequencing in Microprogrammed control unit.	CO2	L2	10M
	OR			
B)	Demonstrate the General Register Organization diagram and explain.	CO2	L2	10M
13. A)	Make use of Booth Multiplication Algorithm to perform multiplication on $-9_{(10)}$ and $-13_{(10)}$.	CO3	L3	10M
	OR			
B)	Draw the flowchart for add and subtract operations.	CO3	L2	10M
14. A)	Explain Programmed I/O with neat flowchart.	CO4	L2	10M
	OR			
B)	Draw the diagram of memory hierarchy and explain auxiliary memory.	CO4	L2	10M
15. A)	Make use of Instruction pipeline to demonstrate the advantage of Instruction pipeline	CO5	L3	10M
	OR			
B)	Explain what is cache coherence problem and how to resolve it.	CO5	L2	10M