Question Paper Code: R22A21EC01

R22

ANURAG Engineering College

(An Autonomous Institution)

II B.Tech. I Semester Regular Examinations, Jan/Feb–2024

DIGITAL ELECTRONICS

(COMMON TO CSE & IT)

Time: 3 Hours **Max. Marks: 60**

Section – A (Short Answer type questions) (10 Marks)

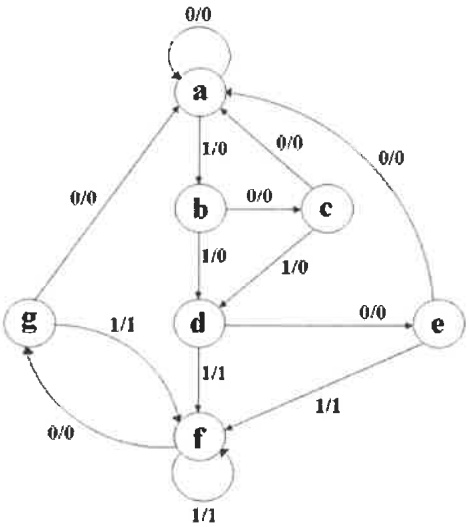
Answer All Questions		Course Outcome	B.T Level	Marks
1.	Apply De-Morgan's theorem to simplify (A+BC)'.	CO1	L2	1M
2.	Convert (115)10 and (235)10 into hexadecimal numbers.	CO1	L1	1M
3.	Show how to connect NAND gates to get an AND gate and OR gate?	CO2	L2	1M
4.	Mention the significance of minimization techniques	CO2	L1	1M
5.	Design Half – adder using only NAND gates.	CO3	L2	1M
6.	Design a 2:1 Multiplexer	CO3	L1	1M
7.	List the differences between Asynchronous and Synchronous circuits	CO4	L1	1M
8.	Realize T Flip Flop using SR Flip Flop	CO4	L2	1M
9.	Compare and contrast static RAM and dynamic RAM	CO5	L2	1M
10.	What is PLD? List their types	CO5	L1	1M

Section B (Essay Questions)

Answer all questions, each question carries equal marks. **(5 X 10M = 50M)**

11. A)	Convert (73889.22)10 into the following number system. i) Binary number, Octal number, Hexadecimal number ii) Subtract (111001)2 from (101011) using 1's complement?	CO1	L2	10M
	OR			
B)	i). Simplify the following expression: Y = (A + B)(A + C')(B' + C') ii). Prove that ABC + ABC' +AB'C + A'BC = AB + BC + CA	CO1	L2	5M 5M
12. A)	i) Design the circuit by Using NAND gates F= ABC'+ DE+ AB'D' ii) Simplify and implementation the following SOP function using NOR gates F(A,B,C,D)= ∑m(0,1,4,5,10,11,14,15)	CO2	L3	5M 5M
	OR			
B)	Reduce the expression f(x,y,z,w)= πM(0,2,7,8,9,10,11,15) .d (3,4) using K-Map	CO2	L3	10M
13. A)	i) Design a full adder. ii) Design a full subtractor	CO3	L2	5M 5M
	OR			
B)	Design a 4-bit Magnitude comparator with the three outputs A=B. A<B, A>B	CO3	L2	10M

14. A)	Design a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible.	CO4	L3	10M



OR

B)	Design a synchronous counter with states 0, 1, 2, 3, 0, 1, ... using JK flip flop	CO4	L3	10M
15. A)	Give the classification of semiconductor memories	CO5	L2	10M

OR

B)	A combinational circuit is defined as the function F1 = AB'C'+AB'C+ABC and F2 = A'BC+AB'C+ABC. Implement the digital circuit with a PLA having 3 inputs, 3 product terms and 2 outputs	CO5	L2	10M