

ANURAG Engineering College
(An Autonomous Institution)
II B.Tech I Semester Supplementary Examinations, June/July-2024
DIGITAL ELECTRONICS
(COMMON TO CSE & IT)

Time: 3 Hours

Max. Marks: 60

Section – A (Short Answer type questions)		(10 Marks)		
Answer All Questions		Course Outcome	B.T Level	Marks
1.	Convert $(47A)_{16}$ to $()_2$.	CO1	L2	1M
2.	Why NAND and NOR gates are called as universal gates.	CO1	L1	1M
3.	What is don't care condition in K Map.	CO2	L1	1M
4.	Draw the 3 variable k map structure.	CO2	L1	1M
5.	Draw the logic diagram of half subtractor.	CO3	L1	1M
6.	What is a multiplexer.	CO3	L1	1M
7.	Mention the types of flipflops.	CO4	L1	1M
8.	What is a register.	CO4	L1	1M
9.	What is ROM. Mention the types of ROM.	CO5	L1	1M
10.	What is Race free state.	CO5	L1	1M

Section B (Essay Questions)

Answer all questions, each question carries equal marks.		(5 X 10M = 50M)		
11. A)	Solve the given Boolean expression using Boolean laws. i) $(A+B)(A+B')=A$. ii) $A(A'+B)=AB$	CO1	L3	10M
OR				
B)	Find the canonical form (SOP & POS) for the given Boolean expression. i) $Y(A,B,C) = A'B'+BC+AC'$ ii) $Y(A,B,C) = (A+C')(A'+B')(A+C')$	CO1	L3	10M
12. A)	Minimize the expression using K-Map i) $Y(A,B,C,D) = \sum m(0,1,2,3,4,5,6,7,11,13,14)$ ii) $Y(A,B,C,D,E) = \prod M(3,4,7,11,15,19,21,23,27,28,29,31)$	CO2	L3	10M
OR				
B)	Implement the following function using NOR Logic i) $Y=AC+BC+AB+D$ ii) $Y = (A'+B)C$	CO2	L3	10M
13. A)	Explain Half adder and Full adder with logic diagram and truth table.	CO3	L2	10M
OR				
B)	Write the verilog module for i) 2 to 4 decoder ii) 4:1 multiplexer	CO3	L2	10M
14. A)	Elaborate on the types of registers in detail.	CO4	L2	10M
OR				
B)	Design a 4 bit synchronous counter using D Flipflop.	CO4	L3	10M
15. A)	A combinational circuit is defined by the function $F1 = \sum m(3,5,7)$, $F2 = \sum m(4,5,7)$. Implement the circuit using a PLA which consists of 3 inputs (A, B and C), 3 product terms and two outputs.	CO5	L3	10M
OR				
B)	Discuss in detail about types of memories.	CO5	L2	10M