ANURAG Engineering College
(An Autonomous Institution)
II B.Tech. I Semester Regular Examinations, Jan–2024
DIGITAL LOGIC DESIGN
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours   **Max. Marks: 60**

Section – A (Short Answer type questions)   (10 Marks)
Answer All Questions

		Course Outcome	B.T Level	Marks
1.	Convert the hexadecimal number 2FC3 into binary.	CO1	L2	1M
2.	List the universal gates.	CO1	L1	1M
3.	Define don't care entries.	CO2	L1	1M
4.	List CMOS logic families.	CO2	L1	1M
5.	What do you mean by latch?	CO3	L1	1M
6.	Differentiate between decoder and encoder.	CO3	L2	1M
7.	What is Ripple Counter?	CO4	L1	1M
8.	Define Modulo counter.	CO4	L1	1M
9.	What is Mealy machine?	CO5	L1	1M
10.	Write about hazards?	CO5	L2	1M

Section B (Essay Questions)
Answer all questions, each question carries equal marks.   (5 X 10M = 50M)

			Course Outcome	B.T Level	Marks
11.	A)	Design and explain 3-bit gray to binary code.	CO1	L3	10M
		OR			
	B)	Two numbers A & B in Hex decimal are given A=85CA, B=23C6. i) Find the decimal equivalent of A & B. ii) Find the binary of A & B. iii) What is sum of A & B in hexadecimal?	CO1	L2	10M
12.	A)	Using K map simplify the SOP function and realize it using NAND gates only. $f(a,b,c) = \sum m(0,2,3,4,5,6)$	CO2	L3	10M
		OR			
	B)	Compare and contrast CMOS logic families.	CO2	L2	10M
13.	A)	Construct a D flip flop in to a JK flip flop showing all the steps.	CO3	L3	10M
		OR			
	B)	Enumerate & explain Architectural Distinctions between Combinational and Sequential circuits.	CO3	L2	10M
14.	A)	Build a synchronous counter using T flip flop to count the following sequence: 0-3-1-4-0.	CO4	L3	10M
		OR			
	B)	Make use of working of a 4-bit twisted ring counter with the help of timing diagrams.	CO4	L2	10M
15.	A)	Describe the state equivalence and machine minimization.	CO5	L2	10M
		OR			
	B)	Illustrate the merge graphs.	CO5	L2	10M