ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Supplementary Examinations, June/July – 2024 DIGITAL LOGIC DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours Max. Marks: 60

	220 420	11200	220 172002 2					
Section – A (Short Answer type questions)			(10 Marks)					
	r All Questions	Course	B.T	Marks				
		Outcome	Level					
1.	What are the Universal gates?	CO1	L1	1 M				
2.	Write the applications of Hamming code.	CO1	L2	1M				
3.	Construct OR gate using diodes.	CO2	L1	1M				
4.	Classify Logic Families.	CO2	L2	1M				
5.	What is the difference between latch and flip flop?	CO3	L1	1M				
6.	Write the truth table of JK flip flop.	CO3	L2	1M				
7.	What is the significance of a shift register in data communication systems?	CO4	L1	1M				
8.	Define the term "modulus" in the context of counters.	CO4	L2	1M				
9.	Define the term "state table" in the context of FSMs.	CO5	L1	1M				
10.	What do you mean by merger graphs?	CO5	L2	1M				
10.	What do you mean by merger graphs.	003	112	1141				
Section B (Essay Questions)								
Answer all questions, each question carries equal marks.		$(5 \times 10M = 50M)$						
	Perform (-50)-(-10) in binary using the signed-2's complement	CO1 `	L3	10M				
	OR							
B)	Develop a Logic diagram for the Boolean function F = A ^l B +AB ^l i) using NOR gates ii) using NAND gates	CO1	L2	10M				
	i) using NON gates ii) using NAND gates							
12. A)	Compare RTL, TTL and CMOS Logic families.	CO2	L3	10 M				
	OR							
B)	With the aid of a four-variable Karnaugh map, derive minimal sum-	CO2	L3	10M				
	of products expressions for each of the following functions.							
	i) $f(A,B,C,D) = \sum m(0,2,4,9,12,15) + d m(1,5,7,10)$.							
	ii) $f(A,B,C,D) = \sum m(1,2,3,5,13) + d m(6,7,8,9,11,15)$.							
12 4)	Involument the following Declary function using 9*1 multipleyer	CO3	L3	101/4				
13. A)	Implement the following Boolean function using 8*1 multiplexer.	CO3	L3	10 M				
	$F(A,B,C,D) = \sum m (2,3,5,7,10,14)$							
77)	OR	CO2	т 2	10% (
B)	Compare combinational and sequential logic circuits.	CO3	L3	10M				
14 4)	Explain the expection of 4 hit DCD country with movelled load	CO4	ТЭ	1014				
14. A)	Explain the operation of 4 bit BCD counter with parallel load.	CO4	L2	10M				
ימ.	OR	CO4	Т 2	101/4				
B)	Design a modulo 5 synchronous counter using JK Flip Flop and	CO4	L3	10M				
	implement it. Construct its timing diagram.							

15. A) Design sequential circuit of Moore model for the fallowing state CO5 L3 10M table.

Present	Next	Output	
state	X=0	X=1	Z
A	A	C	0
В	D	A	0
С	С	A	1
D	В	D	1

OR

B) Explain briefly Moore and Mealy machines? Compare them. CO5 L2 10M