ANURAG Engineering College

(An Autonomous Institution)

II B.Tech I Semester Regular Examinations, Jan/Feb-2024 COMPUTER ORGANIZATION AND MICROPROCESSOR (INFORMATION TECHNOLOGY)

| Time: 3 Hours | | Max. Marks: 60 | | |
|---|---|----------------|-------|-------------|
| Section – A (Short Answer type questions) | | | | Marks) |
| Answe | er All Questions | Course | B.T | Marks |
| | | Outcome | Level | |
| 1. | Define Computer Architecture. | CO1 | L1 | 1 M |
| 2. | What is Instruction Code. | CO1 | L1 | 1 M |
| 3. | Define segment register. | CO2 | L1 | 1 M |
| 4. | What is the advantage of condition code flag register. | CO2 | L1 | 1M |
| 5. | Define OPCODE. | CO3 | L1 | 1M |
| 6. | What is the use of MOVESB instruction. | CO3 | L1 | 1M |
| 7. | What is the use of signed 2's complement representation. | CO4 | L1 | 1 M |
| 8. | Define Isolated I/O. | CO4 | L1 | 1M |
| 9. | What do you mean by parallel processing? How it is achieved using | CO5 | L1 | 1M |
| | pipelining concept? | | | |
| 10. | Define Vector Processing. | CO5 | L1 | 1M |
| | Section B (Essay Questions) | | | |
| Answe | r all questions, each question carries equal marks. | (5) | X 10M | = 50M) |
| 11. A) | Explain different types of basic registers and how they are connected | CO1 | L2 | 10M |
| | to a common bus? | | | |
| 77) | OR | | | |
| В) | Explain about Input-Output Interrupt. | CO1 | L2 | 10M |
| 12. A) | Explain about general bus operation cycle of 8086. | CO2 | L2 | 10M |
| , | OR | | | |
| B) | Illustrate different special processor activities in 8086. | CO2 | L2 | 10M |
| | | | | |
| 13. A) | Write an Assembly Level program to find out decimal addition of | CO3 | L2 | 10M |
| | Sixteen four-digit decimal numbers. | | | |
| | OR | | | |
| B) | Write an Assembly Language program to find out transpose of a 3x3 matrix. | CO3 | L2 | 10M |
| | | | | |
| 14. A) | Illustrate Division Algorithm with an example. | CO4 | L3 | 10M |
| | OR | 004 | 133 | 10141 |
| B) | Explain about Daisy-Chain Priority with interrupt with a neat sketch. | CO4 | L2 | 10M |
| | | | | |
| 15. A). | Explain about memory hierarchy with a neat sketch. | CO5 | L2 | 10 M |
| | OR | | | |
| B) | Explain any two memory mapping methods in cache memory. | CO5 | L2 | 10M |

