

ANURAG Engineering College
(An Autonomous Institution)

II B.Tech II Semester Regular Examinations, June/July – 2024
LINEAR AND DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Time: 3 Hours

Max. Marks: 60

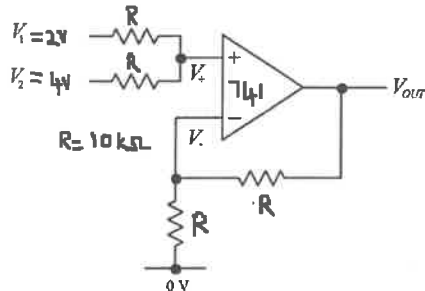
Section – A (Short Answer type questions)

(10 Marks)

Answer All Questions

Course Outcome	B.T Level	Marks
CO1	L1	1M
CO1	L2	1M

- List the ideal characteristics of an Op-Amp.
- Analyze the circuit and calculate the output voltage.



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|---|-----|----|----|
| 3. Summarize the advantages of active filters over passive filters. | CO2 | L2 | 1M |
| 4. Mention any two applications of monostable multivibrator. | CO2 | L1 | 1M |
| 5. Define and calculate the resolution of 8-bit DAC. | CO3 | L1 | 1M |
| 6. Draw the schematic of 4-bit Parallel Comparator Type ADC. | CO3 | L2 | 1M |
| 7. Define noise margin in IC logic family. | CO4 | L1 | 1M |
| 8. Explain how an XOR gate is used as parity checker. | CO4 | L2 | 1M |
| 9. Draw the logic diagram for master slave JK-flip-flop. | CO5 | L2 | 1M |
| 10. Differentiate Static and Dynamic RAM. | CO5 | L1 | 1M |

Section B (Essay Questions)

Answer all questions, each question carries equal marks.

(5 X 10M = 50M)

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|---|-----|----|----|
| 11. A) i) Discuss about the DC characteristics of operational amplifier.
ii) Draw the internal block diagram of an Op-amp and explain about each block in detail. | CO1 | L2 | 5M |
| | CO1 | L2 | 5M |
| OR | | | |
| B) i) Analyze the parameters that should be considered for a.c. and d.c. applications of an op-amp.
ii) Construct the op-amp based circuit to implement the equation $V_o = -5V_1 + 2V_2 - 10V_3$ | CO1 | L3 | 5M |
| | CO1 | L3 | 5M |
| 12. A) i) Build an op-amp based monostable multivibrator to generate a delay of 2ms. (Make necessary assumptions.)
ii) Draw the internal schematic of IC 555 as an astable operation and explain the working. | CO2 | L3 | 5M |
| | CO2 | L3 | 5M |
| OR | | | |
| B) i) A Second -order high-pass filter using a 741 op-amp has $R_1 = 56k\Omega$, and $C_1 = 600 pF$. Calculate the circuit cut off frequency and Obtain its transfer function.
ii) Analyze the circuit of PLL as a frequency multiplier and explain its working. | CO2 | L3 | 5M |
| | CO2 | L4 | 5M |

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|-----------|--|-----|----|----|
| 13. A) | i) Explain the working of dual slope type ADC. | CO3 | L2 | 5M |
| | ii) Evaluate the output voltage of a 3-Bit R-2R Ladder DAC for the digital data of "110" and a gain of unity. | CO3 | L2 | 5M |
| OR | | | | |
| B) | i) Explain the operation of 8-bit successive approximation type ADC with an example. | CO3 | L2 | 5M |
| | ii) Define the following terms:
(a) accuracy (b) Resolution (c) Linearity (d) Conversion time (e) Settling time | CO3 | L1 | 5M |
| 14. A) | i) Design a 4-bit parallel adder/subtractor circuit. | CO4 | L3 | 5M |
| | ii) Compare TTL and CMOS logic families. | CO4 | L2 | 5M |
| OR | | | | |
| B) | i) Design 8x3 priority encoder. Mention it's any two applications. | CO4 | L3 | 5M |
| | ii) Draw and explain the operation of (IC 74LS151) 8x1 multiplexer. | CO4 | L2 | 5M |
| 15. A) | i) Design and explain a synchronous MOD-12 down-counter using J-K flipflop. | CO5 | L3 | 5M |
| | ii) Construct 4-bit universal shift register. | CO5 | L3 | 5M |
| OR | | | | |
| B) | i) Draw the logic diagram of a decade counter and explain its working. | CO5 | L2 | 5M |
| | ii) Draw and explain the architecture of RAM. | CO5 | L2 | 5M |